

**CHIP-LAST EMBEDDED LOW TEMPERATURE
INTERCONNECTIONS WITH CHIP-FIRST DIMENSIONS**

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CHIP-LAST EMBEDDED LOW TEMPERATURE INTERCONNECTIONS WITH CHIP-FIRST DIMENSIONS

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TABLE OF CONTENTS

	Page
ACKNOWLEDGEMENTS	iii
LIST OF TABLES	viii
LIST OF FIGURES	ix
SUMMARY	xiv
<u>CHAPTER</u>	
1 INTRODUCTION	1
Interconnection Needs of System-on-Package	2
Targets and Needs for Next Generation IC Interconnects	3
Current State-of-the-Art Chip-to-Package Interconnections	5
Fine Pitch Interconnections for Chip-Last and Challenges	6
Motivation of Chip-Last	6
Chip-Last Interconnections	8
Challenges for Chip-Last Interconnections	10
Research Objectives and Thesis Organization	11
2 LITERATURE REVIEW	15
Trends in First Level Interconnection	16
Current Fine Pitch Interconnection Technologies	18
Fine Pitch Solder Bumping	19
Fine Pitch Stud Bumping	24
Copper Pillar with Solder Cap	27
Direct Metal-to-Metal Bonding	30
Emerging Alternative Bonding Techniques	34

Adhesives in Electronic Packaging	36
Isotropic Conductive Adhesive	38
Anisotropic Conductive Adhesive	39
Non-Conductive Adhesive	41
3 EXPERIMENTAL METHODS FOR CHIP-LAST INTERCONNECTION	42
Copper-to-Copper Interconnection for Chip-Last Embedding	42
Fabrication Process for Micro-Copper Bumps	44
Insulation Layer	46
Seed Layer and Dog-Bone Layer Deposition	47
Bump Fabrication by Electroplating	49
Design and Fabrication of Test Vehicles	52
Chip and Substrate Layout	54
Fabrication of Dies with Copper Bumps	57
Fabrication of Build-Up Substrate with Cavity	58
Surface Finish using ENIG Process	60
Assembly Process for 30 μ m Pitch Copper Interconnections	63
Thermo-Mechanical Reliability Testing	65
Characterization of Adhesive Bonded Copper-to-Copper Joints	65
Field Emission Scanning Electron Microscopy	66
Energy Dispersive X-Ray Spectroscopy	66
Cross-section Preparation using Ion Polishing	66
Four-Point Probe Measurement	67
4 RESULTS AND DISCUSSION	68
Fabrication of Coplanar Copper Bumps	68
Effect of Lithography and Electroplating on bump Geometry	68

Coplanarity Study of Micro-Copper Bumps	72
Enhancement of Copper-to-Copper Electrical Contact	73
Thermo-Compression Assembly for Adhesive Bonding	76
Material Characterization of Adhesives	77
Thermal Profile for Bonding	80
High Accuracy 30 μ m Pitch Assembly	80
Adhesive Bonding for Complete Embedding of Ultra-Thin Dies	82
Contact Resistance of Single Cu-to-Cu Interconnection	85
Thermo-Mechanical Reliability of Cu-to-Cu Adhesive Interconnects	86
Unbiased Highly Accelerated Stress Test Performance	87
High Temperature Storage Test Performance	90
Effect of Thermal Shock Testing on Copper Interconnections	91
Morphological and Mechanical Properties of Copper Interconnections	101
Diffusion Study of Cu-to-Cu Interface	102
Proposed Hypothesis for Reliable Cu-to-Cu Interconnections	103
5 CONCLUSIONS AND FUTURE WORK	107
Conclusions	107
Recommendations for Future Work	110
REFERENCES	112

LIST OF TABLES

Table 1.1: 2009 ITRS prediction of chip-package substrate interconnection pitch (μm)...	4
Table 3.1: Conditions used on Plasma-Therm PECVD.....	46
Table 3.2: Photoresist NR7-1500 processing conditions.....	48
Table 3.3: Photoresist NR21-20000P processing conditions.....	49
Table 3.4: Composition of copper electrolyte bath.....	50
Table 3.5: Parameters for copper electroplating.....	51
Table 3.6: Etchants used for seed layer removal	52
Table 3.7: Design intent for each test vehicle.....	53
Table 3.8: Details of dies fabricated for TV	58
Table 3.9: Material Properties for core and build-up material.....	59
Table 4.1: Details for ENIG process: bath composition, temperature and time	76
Table 4.2: Measured properties of the NCF.....	79
Table 4.3: Estimated contact resistance values if similar interconnections were made with different materials with similar dimensions.....	86
Table 4.4: Summary of reliability testing performed on each test vehicle	87

LIST OF FIGURES

Figure 1.1: Vision for System-on-Package (courtesy PRC)	2
Figure 1.2: Motivation for Chip-Last.....	7
Figure 1.3: Schematic of an integrated test vehicle for chip-last module.....	8
Figure 1.4: Comparison of chip-last interconnection with chip-first and flip-chip	9
Figure 2.1: Traditional chip-to-substrate interconnection methods	16
Figure 2.2: Transition in microelectronic technology using first level pitch as indicator (based on ITRS projections)	17
Figure 2.3: Evolution of IC Packaging	17
Figure 2.4: Limitations of current solder joint technology at lower pitches.....	18
Figure 2.5: SEM image of cross-section of micro-C4 solder joint at 100 μ m and 50 μ m pitch	20
Figure 2.6: SEM image of cross-section of micro joint formed using CuSn solder and ENIG	21
Figure 2.7: SEM image of cross-section of 25 μ m SnPb solder bumps at 50 μ m.....	22
Figure 2.8: (a) Principle of immersion soldering process (b) SEM image of cross-section of thin solder joint by ISB.....	23
Figure 2.9: SEM image of an Au stud bump (left) un-coined (right) coined	25
Figure 2.10: SEM Image of stud bump at 80m pitch showing open and working connections	25
Figure 2.11: Fabrication process of PI compliant bumps and SEM image of joint formed with ACA on flex.....	26
Figure 2.12: Schematic of C2 flip-chip bump	27

Figure 2.13: SEM image of cross-section of C2 Flip-Chip bump after 1000 TCT	28
Figure 2.14: SEM image of 120um height BoN interconnects.....	29
Figure 2.15: Concept of solder "self-confinement"	30
Figure 2.16: Micro Au bump bonding feasibility with Au, Cu and Al at room temperature.	31
Figure 2.17: SEM of cross-section of a pair of bonded 3um Cu electrodes	32
Figure 2.18: SEM image of copper pillars bonded by electroless plating and annealing. 33	
Figure 2.19: TEM morphology of bonded copper layer between silicon wafers and tantalum barrier layers	34
Figure 2.20: Schematic of phase diagram to explain the basics of SOLID bonding	35
Figure 2.21: Electroless NiB bridge between Cu pads	36
Figure 2.22: Effect of volume fraction of filler on the resistivity of adhesives.....	37
Figure 2.23: Schematic of a flip-chip joint formed by ICA.....	39
Figure 2.24: Method of forming flip-chip joint using ACAs.....	40
Figure 3.1: (a) True stress-strain and cyclic stress-strain (CSS) behavoi of nanocrystalline and microcrystalline copper and (b) Stress-strain curves for solders, copper and Au-Sn braze.....	43
Figure 3.2: Proposed solution for chip-last interconnection	44
Figure 3.3: Fabrication process for electroplated copper micro bumps.....	45
Figure 3.4: Schematic of cross-section of each test vehicle with critical dimensions	53
Figure 3.5: Chip and substrate layout for TV1 depicting Kelvin Probe and Daisy Chain structures	54
Figure 3.6: Snapshot of overlapped die (in red) and substrate (in white) design showing Kelvin Structure and Transconductance Structure	55

Figure 3.7: Chip and substrate layout for TV2 showing the daisy chain structures and cavity wall	56
Figure 3.8: Bump layout and substrate routing design	57
Figure 3.9: Semi-additive metallization on build-up dielectric	59
Figure 3.10: Schematic showing process steps to fabricate cavity on the substrate.....	60
Figure 3.11: Assembly process flow for die embedding using adhesive bonding.....	64
Figure 4.1: Under developed photoresist (PR) leading to defective bumps	69
Figure 4.2: SEM image of defective copper bumps	70
Figure 4.3: Overplated copper bumps leading to mushrooming	71
Figure 4.4: Electroplated micro-copper bumps on silicon at 30 μ m pitch	71
Figure 4.5: SEM image of highly coplanar copper bumps after process optimization.....	72
Figure 4.6: Bump height data for 38 bumps collected randomly from different parts of the wafer	73
Figure 4.7: SEM image of electroless Ni plated on Cu Substrate for 15 minutes	74
Figure 4.8: Copper pads with ENIG after process optimization.....	75
Figure 4.9: Schematic of bonding process using NCF for Flip-chip on Board (FCOB) ..	77
Figure 4.10: Results of DMA for NCF without silica filler.....	78
Figure 4.11: Result of TMA done on NCF without silica filler.....	78
Figure 4.12: Result of DSC analysis performed on the NCF resin.....	79
Figure 4.13: Thermal curing profile used during adhesive bonding.....	80
Figure 4.14: Effect of total length of tool head and die on the assembly yield [54].....	81

Figure 4.15: (a) One metal layer build-up substrate for TV1 (b) 550 μ m thick die assembled on the surface at 30 μ m pitch (b) 55 μ m thick die assembled at 30 μ m pitch ...	82
Figure 4.16: X-ray image showing accurate alignment of 30 μ m pitch copper bumps on substrate pads	82
Figure 4.17: Schematic of assembly process inside a cavity showing proper size of tool head and NCF adjusted for surface roughness.....	83
Figure 4.18: Image of thin die adhesively bonded within the substrate cavity.....	84
Figure 4.19: C-SAM image showing the die-NCF interface after thin die assembly within cavity.....	84
Figure 4.20: SEM image of cross-section of TV2 showing thin die embedded with the substrate	85
Figure 4.21: Contact resistance measurement of single bump by four-point-probe method	85
Figure 4.22: C-SAM images of TV1 under U-HAST test at 0 hour and after 192 hours.	88
Figure 4.23: Change in daisy chain resistance during U-HAST for TV1 at 21N load	89
Figure 4.24: Change in daisy chain resistance during U-HAST for TV1 assembled at 14N load.....	89
Figure 4.25: Change in single bump resistance during U-HAST for 20 bumps across different TV1 assemblies with NCF	90
Figure 4.26: Normalized daisy chain resistance change during HTS for 24 daisy chains	91
Figure 4.27: Daisy chain resistance values under TST for TV1 with 550 μ m thick die ...	93
Figure 4.28: Daisy chain resistance values through 3900 cycles for 30 μ m pitch Cu-Cu interconnections	94
Figure 4.29: SEM image of a highly reliable working daisy chain of Cu-Cu interconnections	95
Figure 4.30: Single Cu-Cu interconnection using NCF.....	95

Figure 4.31: SEM image of a failed daisy chain after 1995 cycles	96
Figure 4.32: Magnified image of a failed bump-pad interface	96
Figure 4.33: Failed daisy chain showing (inset) open connections at bump-pad interface	97
Figure 4.34: Daisy chain resistance data for TV1 with 55um thick dies during TST	97
Figure 4.35: Failures seen in TST before assembly process optimization	98
Figure 4.36: Daisy chain resistance data for TV2 under TST	99
Figure 4.37: 7x7mm ² die assembled on organic substrate using adhesive bonding	99
Figure 4.38: Optical image of the Cu bump on pad with an applied load of (a) 7kg (220MPa) (b) 9.5kg (300MPa)	100
Figure 4.39: TST performance of 7x7mm ² dies under 2 different applied loads for assembly	101
Figure 4.40: SEM image of ion polished copper bump	102
Figure 4.41: Plot of EDS spectra for Cu, Ni and Au obtained across the bump-pad interface.....	103
Figure 4.42: 3D rendered optical image of a deformed substrate pad showing extent of deformation	105
Figure 4.43: SEM image of Cu-Cu interconnection interface under extensive deformation	105

SUMMARY

Small form-factor packages with high integration density are driving the innovations in chip-to-package interconnections. Metallurgical interconnections have evolved from the conventional eutectic and lead-free solders to fine pitch copper pillars with lead-free solder cap. However, scaling down the bump pitch below 50-80 μ m and increasing the interconnect density with this approach creates a challenge in terms of accurate solder mask lithography and joint reliability with low stand-off heights. Going beyond the state of the art flip-chip interconnection technology to achieve ultra-fine bump pitch and high reliability requires a fundamentally- different approach towards highly functional and integrated systems. This research demonstrates a low-profile copper-to-copper interconnect material and process approach with less than 20 μ m total height using adhesive bonding at lower temperature than other state-of-the-art methods. The research focuses on: (1) exploring a novel solution for ultra-fine pitch (< 30 μ m) interconnections, (2) advanced materials and assembly process for copper-to-copper interconnections, and (3) design, fabrication and characterization of test vehicles for reliability and failure analysis of the interconnection.

This research represents the first demonstration of ultra-fine pitch Cu-to-Cu interconnection below 200°C using non-conductive film (NCF) as an adhesive to achieve bonding between silicon die and organic substrate. The fabrication process optimization and characterization of copper bumps, NCF and build-up substrate was performed as a part of the study. The test vehicles were studied for mechanical reliability performance under unbiased highly accelerated stress test (U-HAST), high temperature storage (HTS) and thermal shock test (TST). This robust interconnect scheme was also shown to

perform well with different die sizes, die thicknesses and with embedded dies. A simple and reliable, low-cost and low-temperature direct Cu-Cu bonding was demonstrated offering a potential solution for future flip chip packages and chip-last embedded active devices in organic substrates.

1. INTRODUCTION

Modern electronic packages encompass various possibilities of functional integration to lead to highly convergent mixed-signal microsystems. System on Package (SOP) is a fast emerging concept that addresses the needs of the next generation technology. The key drivers for this technology are heterogeneous integration of microelectronics including wireless, optoelectronics, micro electro-mechanical systems (MEMS) and microsensor functions and integration of these in a single package for mega-functional systems. This concept was pioneered at 3D Systems Packaging Research Center in Georgia Institute of Technology with a vision to facilitate a system level integration including device, package and system board.

Such miniaturization of microelectronic systems needs advanced materials and processes for chip to package interconnections due to the demand for large number of chip-to-chip I/Os at ultra-fine pitches. The move to lead-free solder bonding driven by environmental concerns has increased the chip assembly temperature to 260°C, however, future devices including MEMS, memory and logic circuits are expected to be more sensitive to thermal loads, and the industry has identified a critical need for bonding materials and processes at less than 200°C. This thesis focuses on exploring novel solutions for fine-pitch and low temperature chip to package first level interconnections and demonstrate a reliable interconnection architecture using advanced materials and process methods. This chapter outlines the research objectives of this work derived from the trends in emerging multi-functional electronic systems.

1.1 Interconnection Needs of System-on-Package

The concept of SOP, very often referred to as “second law of electronics” (compare to Moore’s Law for IC’s), strives to integrate the device and system components into a single package through miniaturization and co-design [1]. Over the past few decades, device R&D has made IC’s smaller and highly functional. However, ICs form a small part of the entire system, greater part of the system still needs to converge from millimeter to micrometer scale to nanometer-scale [2]. Future microsystems would not only require microelectronics but also functions like photonics, RF, MEMS, sensors and biological integrated into small form factors resulting in much higher volumetric component density. Advanced building block technologies are thus required in the form of thin film embedded passives using nano-materials, micro-to-nano scale interconnections, thin film embedded batteries, advanced nano thermal interface materials and high density substrate technology for system integration as shown in Figure 1.1.

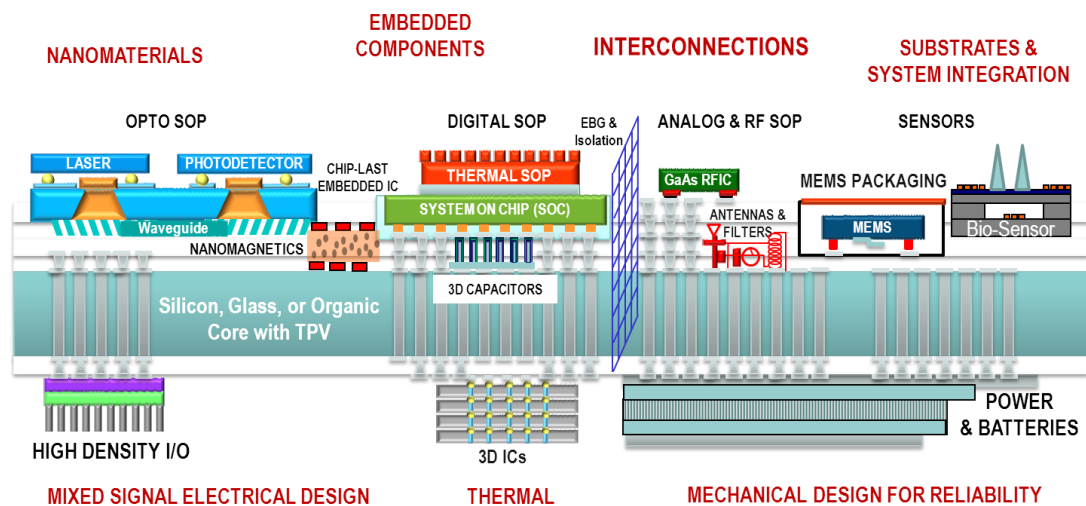


Figure 1.1: Vision for System-on-Package (courtesy PRC)

Integration at chip level has clearly followed Moore's Law [3] which now industry believes to be at 28nm lithography node and headed for 20nm technology [4]. With so called "nano chips" with exceeding billion transistors, I/O requirements of high performance mixed signal IC's are pushing over 10,000 working at power levels of around 150W. These I/Os are being designed to function at a bandwidth of more than 1 terabits per second computing speed for highest system performance [5].

The SOP modules, by definition, will have multiple high performance chips, each having high I/O density for providing power/ground and signal to the module. Such interconnections are projected to be extremely closely spaced down to 1-20 μ m in pitch and ultra-short to have the best electrical performance. Thus, high density interconnections being developed for SOP systems require a paradigm shift from the traditional bulky interconnection technologies used to assemble discrete I/Cs and passive components on board. The integrated systems are envisioned to be extremely thin having multiple dies embedded within the substrate. The interconnections enabling such embedding need to have dimensions an order of magnitude smaller than the existing state of the art solutions.

1.2 Targets and Needs for Next Generation IC Interconnects

The International Technology Roadmap for Semiconductors (ITRS) publishes reports on the current status and projections for almost every aspect of semiconductor manufacturing covering areas from chip design to assembly and packaging. This section derives targets for next-generation chip-to-package substrate interconnections for coming

years from the latest reports published by ITRS [6] and discusses key challenges in developing next generation of high density interconnections.

Table 1.1 summarizes the roadmap for first level interconnections for broad categories in wire bond, flip-chip and chip on film (considered to be an alternative to TAB). The reports also point out that although lower pitch is possible in each of the categories, the cost constraints inhibit going down to lower pitches.

Table 1.1: 2009 ITRS prediction of chip-package substrate interconnection pitch (μm)

Year of Production	2009	2011	2015	2020	2024
Au Wire Bond – single in-line (μm)	35	30	25	25	25
Chip on Film	25	20	10	10	10
Cu Wire Bond – single in-line	50	40	35	35	35
Flip-chip area array	150	120	100	95	95
Flip-chip peripheral	60	50	40	35	35

The flip-chip I/O pitch requirements may vary depending on the application but the predictions shown in the table depicts needs of emerging low cost packages for mobile and portable consumer electronic applications. The I/O pad pitch is predicted to be 20-40 μm accelerated by the adoption of 3D-IC and through silicon via (TSV) technology.

The I/O pad pitch targets have an aggressive roadmap to follow. In conjunction with these targets, the ITRS indentifies that the existing state of the art interconnection

technologies need specific material innovations in assembly and packaging as mentioned below.

- Emerging interconnection technologies need low assembly temperature ($<200^{\circ}\text{C}$). Lead-free solder has long been challenged with its leaded predecessors for higher reflow temperature. To continue using solder based flip-chip joints, advanced solder materials need to be innovated with reflow temperatures less than 200°C .
- As the dimensions of interconnections shrink, better underfill type materials will be needed. Next generation of polymers leading to low CTE (10-14ppm) will be needed. Advanced underfill materials are predicted to have low shrinkage post cure.

1.3 Current State-of-the-Art Chip-to-Package Interconnections:

Innovations in chip-package interconnections and substrates have pushed the microsystems from being large bulky packages to highly compact millimeter scale packages. Standard surface mount technology using flip-chip seems to reach its potential limits of size and efficiency limiting their pitch to 130-150 μm in production today. From the invention of C4 bumps with eutectic Sn-Pb solder by IBM to Pb-free flip-chip solder bumps enforced due to environmental regulations, the interconnection size has shrunk as per the pitch requirements of the package. These solder materials, by nature, have low fatigue resistance and pose challenge towards thermal-mechanical reliability at low stand-off height. This restricts the reduction in pitch of solder joints as tall solder bumps reach their physical limitations.

To further reduce the package size, especially the thickness of the package, and drastically increase the I/O density of the package, chip embedding technologies are being developed as a next generation to flip-chip. Thin embedded chip interconnections enable ~5X reduction in interconnection pitch compared to flip-chip. The chip is connected to the substrate using plated through-via interconnections which has the capability to form short closely spaced interconnection pushing the first-level interconnection pitch further down to 80-100 μ m.

1.4 Fine Pitch Interconnections for Chip-Last and Challenges

Motivation for Chip-Last

Traditional approaches involve embedding the die at the start of module fabrication followed by build-up process by chip-first approach. Another choice of introducing the die in the embedding process is in the middle of substrate fabrication by chip-middle approach. The process for embedding dies in substrate by Shinko is a typical example of chip this approach. While companies are exploring serial processing of die and build-up, Matsushita embeds their passive and active chip in discrete molded laminate layers which are bonded together and connected through inner vias filled with conductive via paste [7].

These conventional embedding processes have several challenges when taking this technology from prototype to volume manufacturing. As the build-up process and routing has its inherent losses during fabrication, it adds up to lower yields after completion of module leaving the embedded dies to be thrown away. Single die packages are not affected by lower yields as much as multi chip packages with expensive silicon and GaAs

dies sitting in single package can go waste. Also testability of functional package becomes a concern owing to functional testing being done at the end of packaging. Process related issues like misaligned micro-vias, warpage of molded panels and die shift during processing looms this technology.

Looking at the roadmap of chip-package interconnections and their evolution, as shown in Figure 1.2, flip-chip justifies the shift from wire bonding and gives a sudden thrust towards high I/O packages with much better electrical performance. However increasing the I/O density using flip-chip becomes a challenge as reducing the pitch creates reliability concerns. Physical constraints to shrink the pitch and size of solder bump create additional concerns. Thus to meet the needs of next generation multi-functional high I/O packages, embedding of die by chip-first approach is done wherein the bond pads on the die are connected to the substrate using micro-via technology which increases the capability of pitch reduction manifold. However this method also creates concerns about process yield.

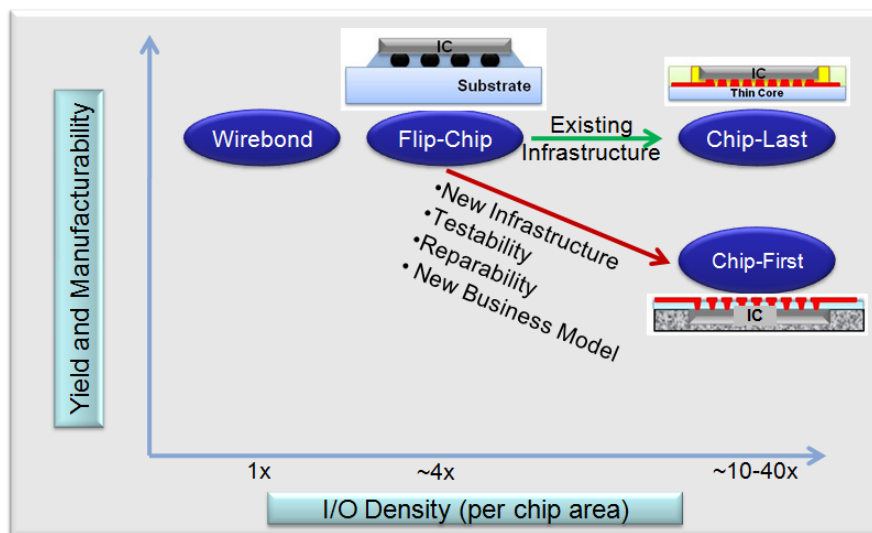


Figure 1.2: Motivation for Chip-Last

3D Systems Packaging Research Center at Georgia Institute of Technology has pioneered a third approach for embedding die called the “chip-last” approach. In this approach, the dies are committed towards the end of substrate module fabrication and testing and embedded in pre-fabricated cavities using thin-film interconnections as shown in the cross-section in Figure 1.3.

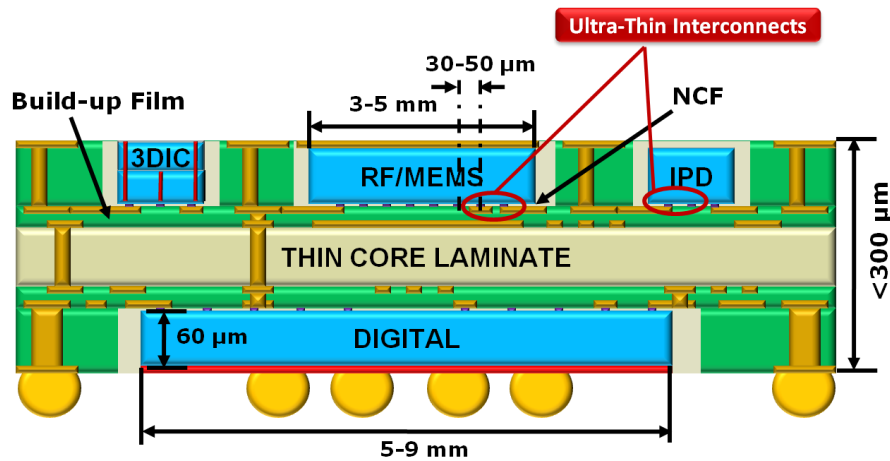


Figure 1.3: Schematic of an integrated test vehicle for chip-last module

Chip-Last Interconnections

Die embedding is conceived as the next generation to flip-chip to achieve the goal of increasing the I/O density by an order of magnitude. Currently die embedding is achieved by chip-first or chip-middle (similar to chip-first) involving embedding the die in a laminate or plastic wafer with active face up followed by thin through-via based interconnections for redistribution. Interconnections for chip-last embedding require dimensions comparable to through-via based interconnections in chip-first like modules to achieve similar I/O density. This also means that the interconnections need to be 5-10X smaller in dimensions as compared to existing flip-chip technologies in order to achieve ultra-fine pitch (30-50μm) interconnections as shown in Figure 1.4.

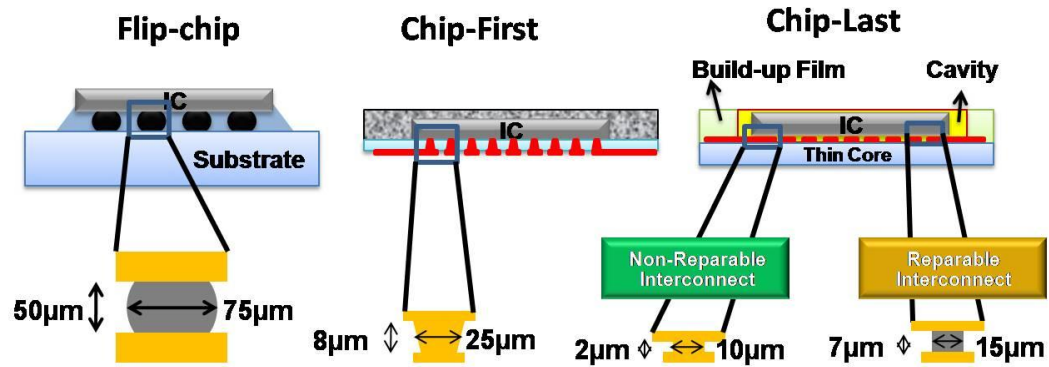


Figure 1.4: Comparison of chip-last interconnection with chip-first and flip-chip

This interconnection approach adopts simple, low cost processes which can be integrated to the existing manufacturing infrastructure easily and possesses the potential for higher yields than chip-first approach while maintaining similar I/O densities. Some of the key advantages derived from chip-last along with the benefits of chip-first are:

- (1) Substrate module can be tested before commitment of die
- (2) Double-side processing of routing wires connected by through-package-vias
- (3) Chip-to-package interconnections at ultrafine pitch with chip-first like dimensions
- (4) Extremely low thickness of final module, as low as 0.3mm thickness.
- (5) Effective heat management with exposed top surface of die.
- (6) Heterogeneous integration of multiple ICs of different thickness.
- (7) Minimal changes to manufacturing infrastructure.

Chip-last technology is projected to have high integration capability with high I/O logic IC being placed with 3D stack of memory ICs on same package with embedded passive components. The core building-blocks which are being developed for functional demonstration of this technology include:

- (a) High wiring density build-up substrate with cavity

- (b) Ultra-fine pitch chip-to-package interconnections
- (c) Embedded passive components

Challenges for Chip-Last Interconnection

Solder bumping the dies for flip chip has strong advantages when compared to its wire-bonded predecessors like flexibility to go from peripheral to a square grid array of I/Os and better electrical performance. However, as the bump pitch reduces it creates excess thermo-mechanical stresses and strains in the silicon to organic substrate first level interconnect. Thermal cycling reliability, varying roughly as the third power of bump diameter is therefore tremendously compromised. As the semiconductor industry is rapidly adopting restriction of hazardous substance (RoHS) compliance, the high reflow temperature of Pb-free solders make the solder process more challenging for organic substrate packages. Moreover electro-migration stress and voiding concern prevails at finer pitches [8]. These concerns have led to development of alternative bump metallurgies with advanced UBM to enable pitch reduction without compromising fatigue life of the joints. Copper based first level interconnections have emerged as a very important bumping technology in recent years because of the following reasons:

- (1) Copper has excellent electrical conductivity and mechanical stability compared to solder
- (2) As copper does not melt at bonding temperature, high I/O density can be achieved with excellent mechanical integrity
- (3) Copper pillar bumping can be easily integrated with back-end manufacturing processes with capability of downscaling from millimeter to nanometer scale.

Several methods of joining copper to copper for establishing electrical connection between silicon die and organic package substrate have been discussed earlier. The most widely used method is by mating solder caps, like eutectic Sn-Pb or Sn-Ag-Cu, to the copper pillar followed by reflow to connect to substrate pads. This method poses limitations towards reduction in bump pitch due to solder mask requirements and reliability of solder [9]. Other methods call for either complex surface preparation or high temperature annealing creating a bottleneck towards manufacturability.

In summary, ultra-fine pitch interconnection for chip-last need a robust solution which maintain a low profile with excellent fatigue life. The fabrication of such interconnections should be easily scaled down to lower dimensions with ease of processability.

1.5 Research Objectives and Thesis Organization

The key objective of this research is to explore, engineer and demonstrate high I/O density chip-to-package interconnections by exploring innovative processes and materials to realize ultra-thin copper-to-copper interconnections. This study is targeted to drive the interconnection needs of die embedded packaging by “chip-last” approach which possesses a potential to reach extremely high I/O densities with low stand-off height ($\sim 10\text{-}15\mu\text{m}$) at par with the state of the art fan-out wafer level packages and substrate embedded packages. Low temperature of processing is one of the key highlights for this technology which makes it an attractive option to go beyond the flip-chip. Long term goals for this research are to form extremely fine pitch ($< 10\mu\text{m}$) pad-to-pad interconnections using thin film metals to form metallurgical interface. This interconnection technology is envisioned to be integrated with wafer level back-end

manufacturing infrastructure and deploying nano-scale thin film processes to fabricate high throughput interconnections at low cost.

As mentioned, low temperature bonding using advanced adhesive materials will be explored to achieve copper-to-copper interconnection. The focus of this thesis will be on (1) Fabrication and characterization of copper bumps at ultra-fine pitch (30-50 μ m), (2) Assembly process optimization for copper-to-copper interconnections, and (3) Reliability and failure analysis of the interconnection. Nonconductive adhesive and nano anisotropic conductive adhesive will be used in the form of thin films to bond chip to substrate. Highly coplanar electroplated copper bump fabrication process will be developed with desired geometry. The assembled packages will be studied for reliability under Unbiased Highly Accelerated Stress Test (U-HAST), High Temperature Storage Stress Test (HTS) and Thermal Shock Test (TST). Extensive failure analysis will be conducted throughout the process of reliability testing to understand the possible modes of failure for this interconnection technology and optimize the materials for excellent performance. The thesis has been divided into six chapters including an introduction to the research enumerating some of the key motivations and advantages behind pursuing this study.

Chapter 2 is dedicated towards identifying the requirements and key R&D challenges for the next generation of first level interconnection technology considering the roadmap for emerging microelectronic systems. At the current pace of evolving ICs, first level interconnection between chip to package has tremendous pressure to shrink the dimensions and pitch. This chapter will cover a detailed discussion on various fine pitch technologies that are being pursued in research and volume manufacturing around the world. The discussion will start with traditional solder bump technology and its

limitations as we go to finer pitches and present alternative methods to achieve interconnection with equal or better electrical and mechanical performance, ease of processing, electromigration resistance and cost. Electrically conductive adhesives (ECAs) and nonconductive adhesives have emerged as an attractive and viable option for lost cost packages. This chapter will also focus on various types of adhesives used in electronic industry along with their advantages and disadvantages.

Chapter 3 involves a discussion on the experimental methods used through the course of research. Considering the key objectives for this research, processes involved in fabrication of optimized copper bumps will be presented. The discussion will also briefly cover the fabrication process of ultra-thin build-up substrates and NCF and nano-ACF which form the building blocks of the test vehicles. Design of various test vehicles used to study the robustness of the interconnection architecture will be shown with details of key features incorporated in the design. This chapter will close with discussion on steps involved in assembly process, reliability testing and methods used to identify failures in the package.

Chapter 4 leads into the results obtained at every step of this study and discussion on findings of the experiment. This section will show all the achievements of the research with regards to fabricating 12-13 μ m electroplated copper bumps with high coplanarity. Optimized assembly process for embedding 55 μ m thin silicon die completely within the cavity on an organic substrate and reliability performance of these packages.

Chapter 5 present derived conclusions and present it coherently aligned to the objectives of the research. The section highlights the demonstration of an advanced interconnection solution to embed ultra-thin silicon dies in organic packages maintaining extremely low

stand-off height. Chapter 6 extends this discussion to close with some comments on the on-going work in this research and scope for improvements and exploring more ideas in this field of research.

2. LITERATURE REVIEW

System level perspective of modern microelectronic environment was presented in the previous chapter. Emerging microelectronic packages are bound to have a more rigorous approach towards system level integration requiring innovative solutions in terms of design, manufacturing technology, tools and materials. Traditional approaches towards packaging will need to be fundamentally redesigned or altered to cope with the requirements of multi-scale systems. As the requirements of assembly and packaging become more stringent, chip-to-package interconnection technology will become the key cornerstone for highly converged miniaturized microelectronic systems. Breakthrough in materials, processing technology and design will be needed to address the needs of these highly complex systems.

This chapter will capture three key aspects of exploring a new fine pitch interconnection technology as we transition from standard surface mount technology (SMT) to embedded systems. Firstly, based on the roadmap for off-chip interconnection technologies, the bottleneck in advancing this technology further and material process requirements for next generation of interconnections is identified. This discussion will lead to an exhaustive survey of state-of-the-art in fine pitch interconnection technologies both in research and manufacturing while presenting materials, process and manufacturing challenges in the existing technologies.. Brief discussion on adhesives used in realizing low temperature interconnections will conclude the chapter.

2.1 Trends in First Level Interconnection

First level interconnections are meant to provide electrical path between the chip and the substrate which are then connected to board via second level interconnections. For the last two decades ICs have been assembled on package substrate using three main approaches: (a) wire bonding the chip with active side up (b) TAB with either active side up or down (c) and flip-chip with active side down as illustrated in the Figure 2.1.

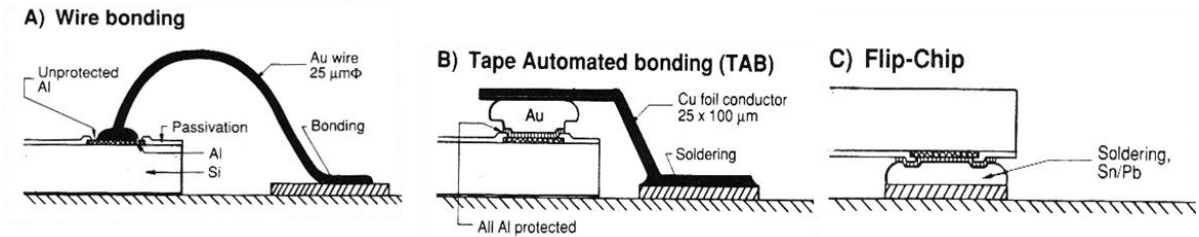


Figure 2.1: Traditional chip-to-substrate interconnection methods [10]

However, with rapid device downscaling and higher I/O requirements for the package, first level interconnections have evolved to accommodate more stringent space and performance requirements. Novel interconnection schemes involving deposited thin films [11], G-shaped springs [12] and laser deposited conductors [13] have been proposed and demonstrated for realizing chip-to-package interconnections. The I/O pad pitch is shrinking at a much faster rate than ever to accommodate the billions of transistors which are now made on a single chip. The fine pitch wire bond technology and flip chip technology are now manufactured down to 80-50 μm and are projected to go well below 20 μm in order to cope up with the demand on IC front end side as shown in Figure 2.2 [6]. The end goal of these fast evolving technologies is to enable high degree of integration in terms of functionality and electrical performance simultaneously.

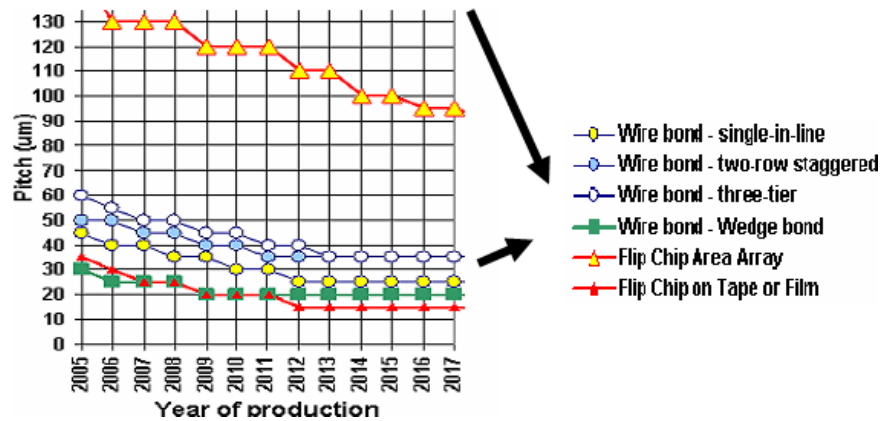


Figure 2.2: Transition in microelectronic technology using first level pitch as indicator (based on ITRS projections)

Figure 2.3 depicts the trend towards highly integrated wafer-level solutions for IC packaging which need greater than 100,000 I/O per cm^2 . Various rigid and compliant interconnection solutions are being developed for wafer level system integration which could potentially push the pitch to 1-5 μm range.

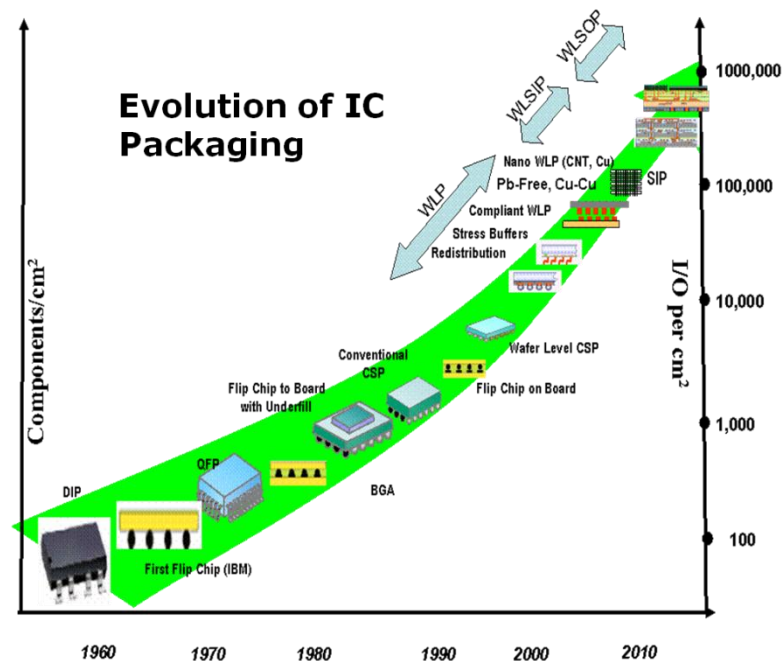


Figure 2.3: Evolution of IC Packaging

2.2 Current Fine Pitch Interconnection Technologies

Since the invention of flip-chip, C4 solder bump technology pioneered by IBM has been the work horse for the industry which is slowly and steadily transforming from wire bond era. The solder bump technology has several advantages given that the material properties of solder and its behavior in various conditions have been well researched and reported. Moreover they are more accommodating towards non-planar substrates and are therefore ideal for organic packages. However, following the interconnection technology roadmap, the solder joint technology is posed by several challenges as the emerging packages demand interconnections at finer pitch. Shrinking the pitch of solder joints poses a physical limitation at similar stand-off height and reliability concern due to low fatigue resistance at lower stand-off heights as shown in Figure 2.4.

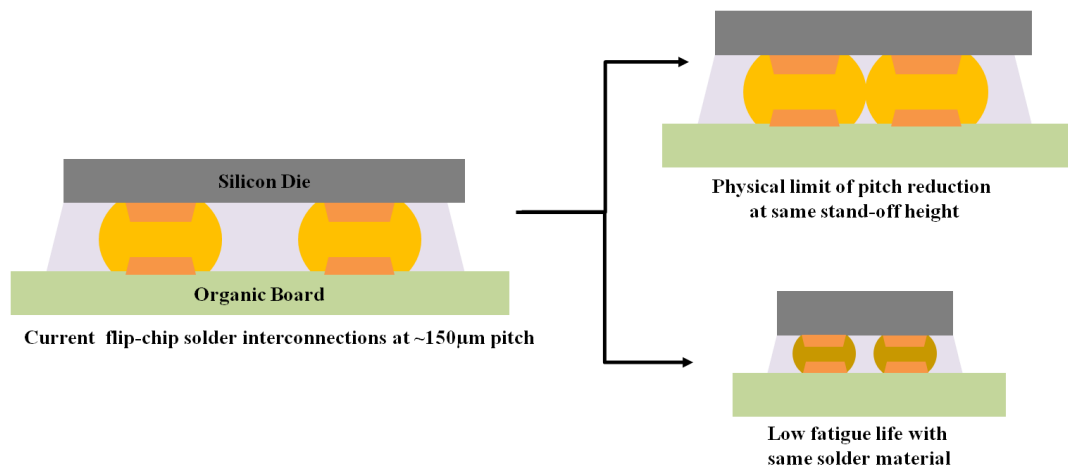


Figure 2.4: Limitations of current solder joint technology at lower pitches

This section enlists various first level interconnections technologies which are in mass production or in R&D and identifies key attributes of each technology and challenges associated with them. The section is divided into four broad categories including (a) solder bump technology, (b) stud bump technology, (c) copper pillar with solder

technology and (d) direct metal-to-metal bonding technology, to cover all the interconnections methods systematically.

2.2.1 Fine pitch Solder Bumping

Solder bumping the IC has been achieved by various methods like electro-deposition of eutectic solder, stencil printing of solder paste and shooting solder balls on the die. Flip-chip interconnections from chip to organic package using solder bumps are at 80-150 μ m bump diameter with 200-250 μ m pitch. Large CTE mismatch between the silicon and organic substrate induces excessive strain on the solder joints as the pitch and size decreases. However, recent advances in fabricating solder joints at finer pitches have been demonstrated for making a 3D stack of ICs by attaching silicon to silicon.

Stacking ICs with 3D interconnections supported by through-silicon-via (TSV) technology is gaining importance for variety of applications including memory stacking, integration of memory with logic ICs and heterogeneous integration of multi-function ICs. These high density TSVs need off-chip interconnection at similar pitch and dimensions for maximum benefit. IBM has developed micro-C4 interconnection for such capability [14]. The μ -C4 solder bumps are fabricated by plated-through resist process which enables significant reduction in solder volume. The μ -C4 solder joining process has been demonstrated for silicon-silicon attached at 50 μ m and 100 μ m pitch with solder diameter of 25 μ m and 50 μ m as shown in Figure 2.5. The process was established for various solder compositions including high-melt solder, PbSn (97/3), eutectic PbSn (37/63), Pb-free solder (Sn/Ag/Cu) and AuSn (80/20). Ball limiting metallurgies (BLM) were also studied for combinations such as TiW/CrCu/C/Ni/Au, Cr/CrCu/Cu/Au,

Ti/Cu/Ni/Au and Ti/Cu/Cr/Cu/Cu/Ni/Au. Single bump DC resistance values were extracted to compare the results from different BLMs at both 100 μ m and 50 μ m pitch [15].

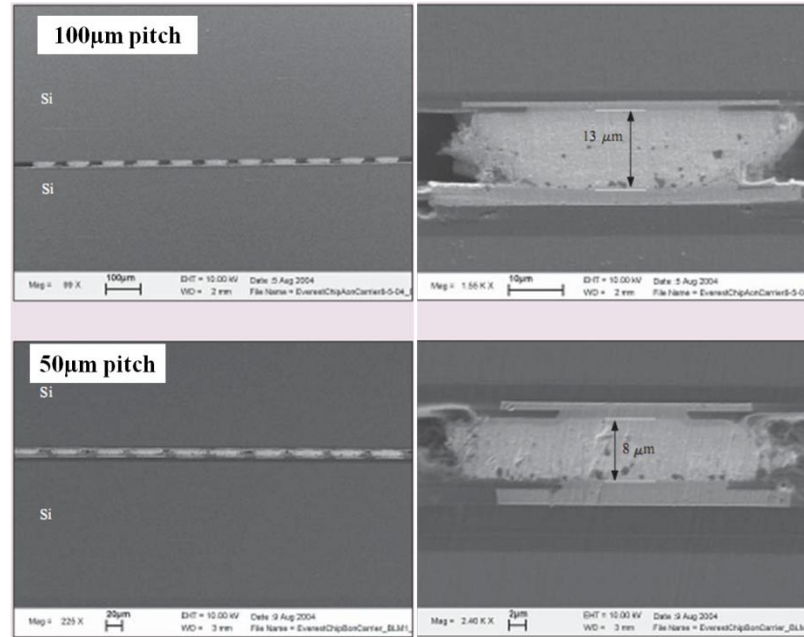


Figure 2.5: SEM image of cross-section of micro-C4 solder joint at 100 μ m and 50 μ m pitch [15]

Similar technology is being developed by Institute of Microelectronics, Singapore for enabling high density 3D systems integration at 15 μ m pitch. Simple through resist plating methods used to electroplate Cu/Su bumps on silicon while the other side of the connection is made through ENIG grown pads as shown in Figure 2.6.

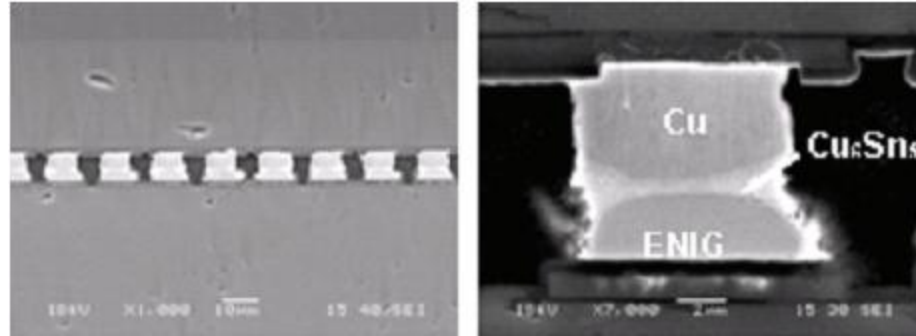


Figure 2.6: SEM image of cross-section of micro joint formed using CuSn solder and ENIG [16]

Such micro joints have also been demonstrated for C/Sn solder micro joined to another C/Sn solder. The assembly process is done at 300-350°C within 1 minute with an applied pressure of 20MPa [16].

Another strong contender for fine pitch solder bump interconnection technology is the Sn/Pb solder bumping process developed by MCNC (Research Triangle Park, NC). The process is capable of fabricating solder joints at 50µm pitch with 25µm bump diameter. These tailored interconnections, shown in Figure 2.7 were developed to allow construction of multi-chip modules of sensor-readout circuit pairs. This process relies on an electroplating method to form the solder bumps, which gives tremendous flexibility in processing conditions and excellent wafer level uniformity. Fine pitch flip chip assembly often creates several issues associated with flux residue removal after reflow. This problem was completely eliminated here by the use of Plasma Assisted Dry Soldering (PADS) process during assembly. PADS is a plasma treatment process that reacts with the tin oxides on the surface of Sn-bearing solders. The tin oxides are converted into a compound that breaks up as the solder melts during reflow, exposing unoxidized solder to the bond pad and allowing complete solder wetting. Reflow is done in a conventional

nitrogen-purged belt furnace that prevents the re-oxidation of the solder during the bonding process [17].

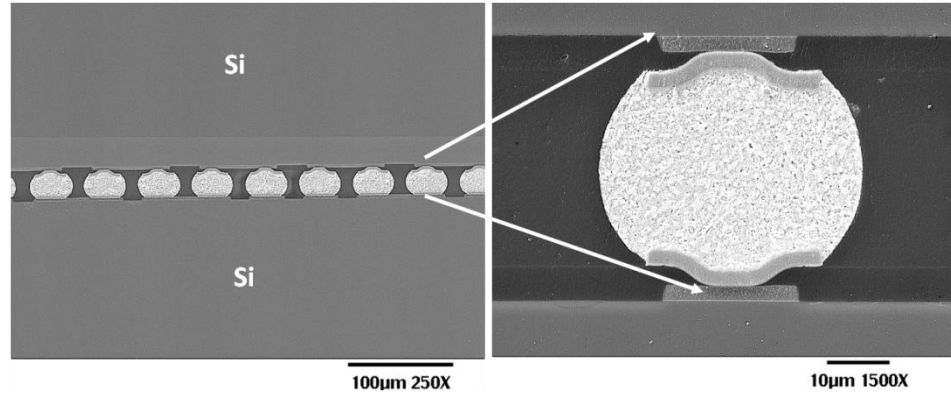


Figure 2.7: SEM image of cross-section of 25μm SnPb solder bumps at 50μm [17]

Fine pitch interconnection technologies are also of interest for attaching thin silicon chip to flexible substrates. Such packages are becoming useful for applications such as smart cards, smart labels and folded packages. Fraunhofer Institute for Reliability and Microintegration in Germany has demonstrated thin solder based interconnections with less than 10μm stand-off height through immersion soldering process providing a low-cost alternative to electroplating process [18]. In this process, the wafer with UBM is completely immersed in the liquid solder maintained at 20-30°C higher than its melting point. Since the solder has excellent wetting characteristics for the UBM, it forms a thin layer on the UBM. This process is illustrated in a schematic in Figure 2.8(a). Thermode bonding was shown as a promising fast flip chip technology for thin soldered contacts on flexible substrates as shown in Figure 2.8(b). Two different solder materials in combination with no-flow underfill materials were studied for flip chip contacts of less than 10μm height. Since the reliability of thin solder joints is a key issue, the failure mechanisms and the ageing behavior were described [18].

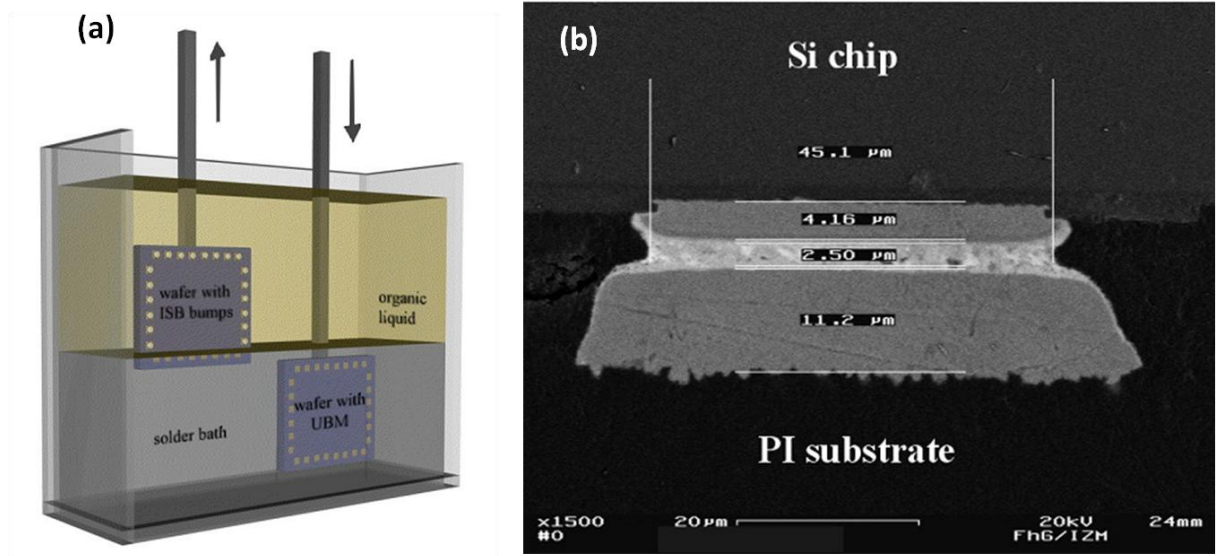


Figure 2.8: (a) Principle of immersion soldering process (b) SEM image of cross-section of thin solder joint by ISB

Another approach for attaching chip to flexible printed circuit board (FPCB) is by electroplating solder bumps on the flexible board for a roll-to-roll process. This method is being pursued at Korea Institute of Industrial Technology and is targeted towards increasing the productivity of the roll-to-roll process. To prevent warpage due to high temperature bonding the solder bumps are made of Sn-58Bi with 35 μm diameter and 75 μm pitch. The measured shear strength for such modules has been reported at 35-30 gm per bump [19].

Clearly, fine pitch solder joints create challenges towards processing and reliability. Solder paste deposition through silk-screen for bumping reaches its limitation at around 150 μm pitch due to rheological limitations of forcing a semi-solid (paste) into small holes (silk screen). Evaporation of solder through metal masks does not meet the cost target and printing it through a stencil in the form of paste can create bump uniformity issues at lower pitches. Apart from processing challenges, reliability becomes a concern for chip-

to-organic substrate interconnection at finer pitches along with several other process related challenges such as difficulty in flux residue cleaning and underfilling due to low stand-off height. Thus, novel architectures and methods are needed to realize chip-to package interconnections at pitches lower than 80-100 μm .

2.2.2 Fine Pitch Stud Bumping

New environmental regulations in most of the countries today prohibit the use of leaded components in the electronic products. This compliance has a direct implication on the solders used for flip-chip attach as lead-free solders which have higher reflow temperatures create greater issues with UBM and pitch reduction . Thus alternative techniques and metallurgies are needed to address these issues. Flip-chip assemblies can also be formed using stud bumps made of gold or copper and attached to organic substrates by thermosonic bonding, thermo-compression bonding or ultrasonic bonding. The gold stud bumps are formed by bonding gold wire to the substrate with force, heat and ultrasonic energy and then snipping the wire just above the formed ball to leave a stud. Companies like Infineon and Texas Instruments are now using this technology in production [20].

Infineon Technologies have studied extensively the reliability of un-coined and coined stud bumps (shown in Figure 2.9) fabricated from gold wires at 60 μm and 80 μm pitch. The study shows that fine pitch stud joints are highly dependent on the X-Y alignment and bump coplanarity. Un-coined bumps keep lower bonding force but are more prone to misalignment compared to coined bumps.

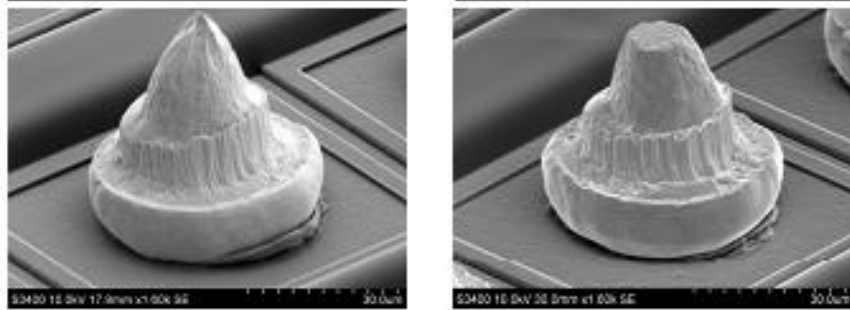


Figure 2.9: SEM image of an Au stud bump (left) un-coined (right) coined [21]

The bonding was achieved by thermo-compression in which the gold stud is made to touch solder coated copper pads which wets the stud surface to make connection. Non conductive polymer (NCP) is dispensed as a no-flow underfill to fill the gap between the chip and substrate as shown in Figure 2.10 [21].

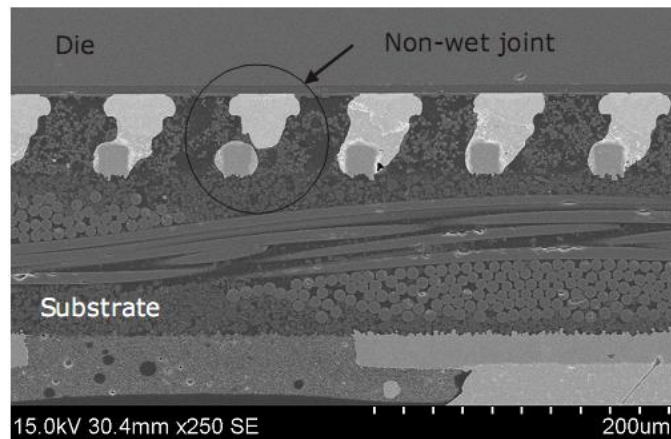


Figure 2.10: SEM Image of stud bump at 80m pitch showing open and working connections [21]

A variation of stud bumping to improve reliability and probe testing capability has been developed by ITRI, Taiwan. To address the issue of bump non-co planarity, compliant bumps are fabricated by using polyimide (PI) as the core of the bump with gold coated on the surface of the bump.

The bumps are partially coated with gold as shown in Figure 2.11 to prevent bridging of two neighboring bumps during flip-chip assembly using anisotropically conductive adhesive (ACA) [22].

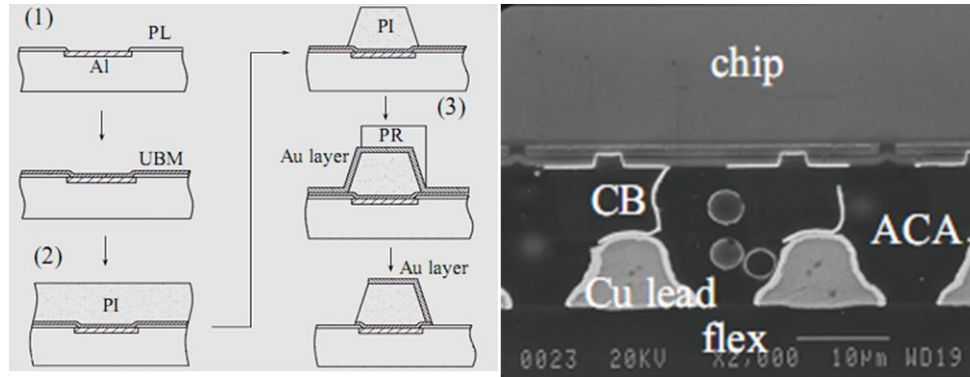


Figure 2.11: Fabrication process of PI compliant bumps and SEM image of joint formed with ACA on flex [22]

In summary stud bumps provide a good alternative to form fine pitch area array interconnections with existing infrastructure like modified wire bonders for bumping the wafers. Such interconnections have been shown to work well with chip on flexible substrates. However from the manufacturing stand point, expensive gold bumps can become a bottleneck for low cost embedded packages. Bump coplanarity is a critical factor for high yield in this technology. Approaches used for addressing this challenge require multi-step processes which should be done at high precision due to alignment concerns. These innovative approaches pose potential to improve the yield and reliability of the process but become a challenge for integration at high volume production.

2.2.3 Copper Pillar with Solder Cap

This technology was pioneered by Intel 10 years back [23] with a vision to overcome the barriers of processing and challenges related to reliability performance challenges with

solder bump joints at pitches finer than 150 μ m. The interconnection between the chip and substrate is established through a copper pillar attached to the substrate via intermediate solder layer. Different solders have been investigated for this purpose but Sn-Ag based solders have sprung as prominent contenders for this technology [24].

IBM calls this technology as C2 flip-chip interconnection – a successor to their C4 technology designed for its Solid Logic Technology (SLT) and still being widely used for processor packages in personal computers (PCs) and games [25]. A schematic of C2 flip-chip bump is shown in Figure 2.12.

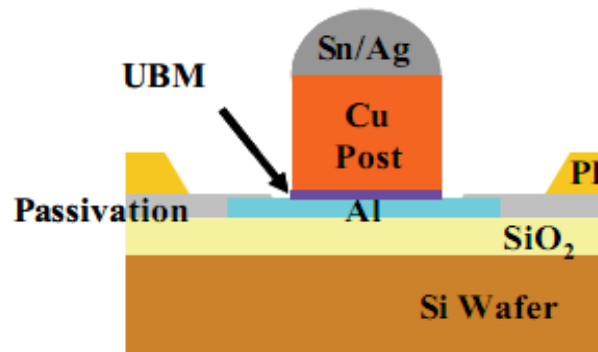


Figure 2.12: Schematic of C2 flip-chip bump [25]

C2 bumps are fabricated by sputtering Ti and Cu as UBM followed by through-resist electroplating of copper post and solder cap. Chip is assembled on the substrate with pre-applied no-clean flux using pick-and-place tool followed by mass reflow to form solder joints. This architecture is capable of supporting fine pitch area array interconnection. IBM has demonstrated reliability of such interconnections under various JEDEC level testing for chips assembled at 80 μ m and 50 μ m pitch. As the device size shrinks low-k and extra low-k dielectric materials for supporting copper redistribution are being investigated to reduce the RC delay. These dielectric materials are mechanically brittle

with low modulus and poor adhesion properties. Thus increasing the silicon die size with fine pitch interconnections aggravates the stresses in the low-k dielectric and needs thorough study with any new interconnection architecture at fine pitch. Aggressive reliability testing was performed for C2 bumps fabricated on low-k devices at 60 μ m pitch. The packages passed MSL3 preconditioning with 3X reflow at 260°C peak temperature and more than 1500 thermal cycles (-55°C to +125°C, 2CPH). The cross-section of a working joint after 1000 thermal cycles is shown in Figure 2.13.

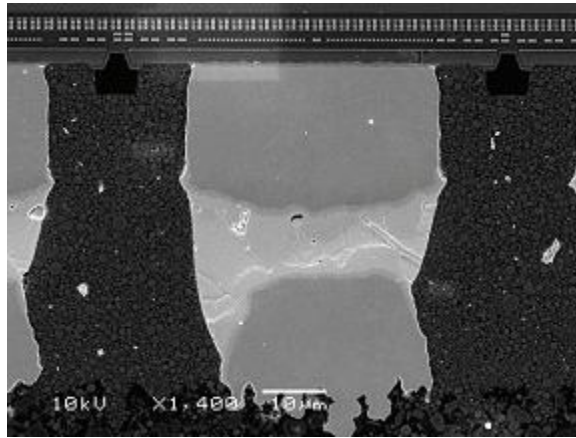


Figure 2.13: SEM image of cross-section of C2 Flip-Chip bump after 1000 TCT

Several companies like Texas Instruments, Advanced Micro Devices, Tessera, Advanpac Solutions and StatsChip Pac are now trying push this interconnection technology towards commercialization at around 80-150 μ m pitches with solder metallurgies based on Sn-(2-3.5wt %) Ag [26-30]. High aspect ratio copper pillars with solder cap have also been investigated by Institute of Microelectronics, Singapore for developing high I/O area array flip-chip interconnections. High aspect ratio (>2) leading to high stand-off height provides compliance to the interconnect structure. Bumps of ~120 μ m height were fabricated by electroplating through thick negative photoresist (JSR THB-151N) which

was optimized for high aspect ratio lithography. The structure also called Bed of Nails (BoN) is shown in Figure 2.14.

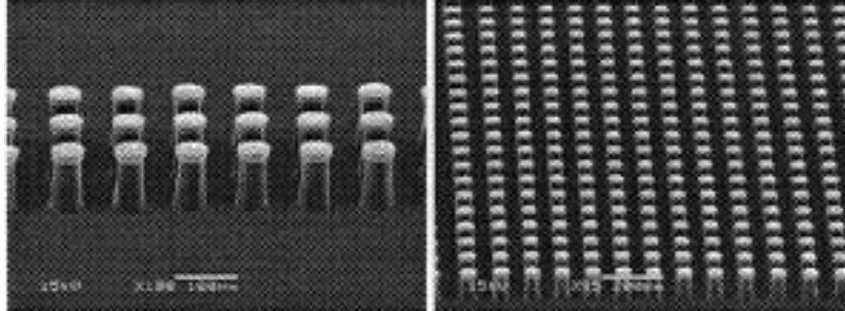


Figure 2.14: SEM image of 120um height BoN interconnects

Copper pillar bumping process provides an excellent alternative to standard solder bumping process for further pitch reduction. However it does not get rid of the solder completely leading to several concerns: (a) bonding temperature dependence on lead-free solder (b) solder mask lithography at finer pitches (c) bump reliability due to electromigration at pitches lower than 50 μm . Several research studies are currently under progress to optimize the bump geometry and solder cap material to push this technology towards finer pitches with high reliability. One of such novel ideas was demonstrated by Pendse *et al.* who designed the bump and solder cap in such a way that the substrate pads with smaller dimension formed a “self-confined fillet” to entirely contain the solder within the joint. As a result, the design rules for substrate routing are relaxed and the need for solder mask is eliminated as illustrated in Figure 2.1 [28].

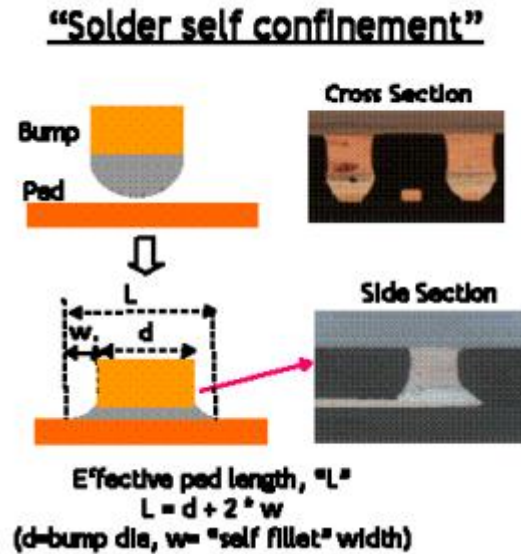


Figure 2.15: Concept of solder "self-confinement" [28]

2.2.4 Direct Metal-to-Metal Bonding

Pure metals like copper and silver are known to have better electrical conductivity than solders [31] and forming off-chip interconnections with good mechanical integrity using them can lead to several benefits like lower contact resistance, lower RC delay and better thermal management. However owing to high melting point for most of the metals used in electronics industry today, processing them like solders for realizing metallurgical interconnections is difficult. Alternative approaches are being investigated for bonding chip to substrate or another chip at extremely high interconnection density. Some of the emerging approaches are listed below:

Surface Activated Bonding

Surface activated bonding (SAB) is based on the concept that two atomically clean surfaces when brought in close contact (due to extremely fine surface roughness) can generate strong cohesive force towards each other. The bond strength can be significantly improved by annealing leading to diffusion across the interface. Suga *et al.* reported

extensive study on feasibility of SAB as off-chip interconnects for chip-on-chip and chip-on-flex system [32]. The study reports interconnection feasibility at room temperature and low temperatures for micro Au bumps with Au, Cu and Al surfaces. Single bump electrical resistance of $7\text{m}\Omega$ and die shear strength of above 5kgf was reported with all the joints. The bonding feasibility of micro Au bumps with Au, Cu and Al is found to be different as shown in Figure 2.16. The surface chemical composition, hardness of mating materials and film thickness are suggested to be important factors contributing to the bonding other than the intermetallic phases formed between them [32].

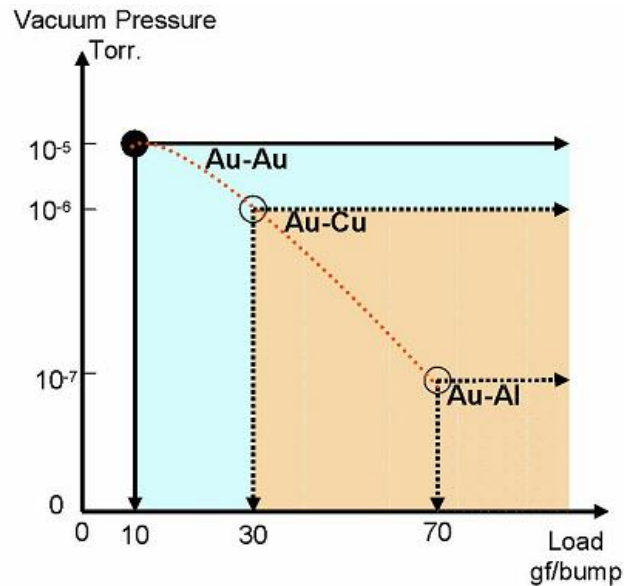


Figure 2.16: Micro Au bump bonding feasibility with Au, Cu and Al at room temperature. [32]

This concept has been used to form ultra-fine pitch chip-to-chip interconnection using bumpless interconnect method. Shigetou *et al.* have reported feasibility and demonstration of chip-to-chip interconnection at $6\text{-}10\mu\text{m}$ using SAB method. The copper wires on the chip face are interconnected using thin copper pads which have undergone chemical mechanical polishing (CMP). The copper plating on chip is done using

damascene process which is normally used for back-end-of-the-line (BEOL) copper redistribution. The CMP-Cu films on the chip have surface roughness of 1-2nm which enables close contact of surfaces. The interconnection can be considered as pad-to-pad bond due to very small gap between the bonded chips as shown in Figure 2.17. These high density interconnections were tested for reliability under thermal aging test at 150°C for 1000 hours showing marginal increase in contact resistance for 100,000 bumpless electrodes [33].

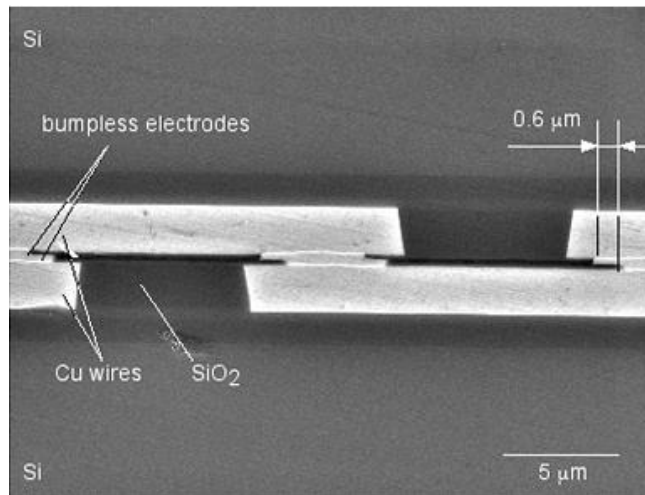


Figure 2.17: SEM of cross-section of a pair of bonded 3μm Cu electrodes [33]

Copper-to-Copper Electroless Plated Pillar Interconnects

A He *et al.* has studied and reported another method of joining pure copper to copper for chip-to-substrate interconnections. In this all-copper process, copper is electroplated as pillars on chip and substrate using through-resist electroplating. Subsequent to this, the two pillars are flip-chip aligned and temporarily held at a fixed distance with each other. The joint is then established by electroless plating of copper until the two surfaces are in intimate contact. The bond strength of the entire structure is improved by annealing at 180°C to 400°C in nitrogen environment. The interconnect structure, similar to the one

shown in Figure 2.18, possesses a shear strength of 165MPa compared to yield stress of bulk electrodeposited copper is on the order of 225MPa [34]. This method addresses the problem of non-co planarity in direct copper-to-copper bonding which becomes an issue in SAB technique. However post anneal requirements in this method create a challenge for integration with PCB type processes.

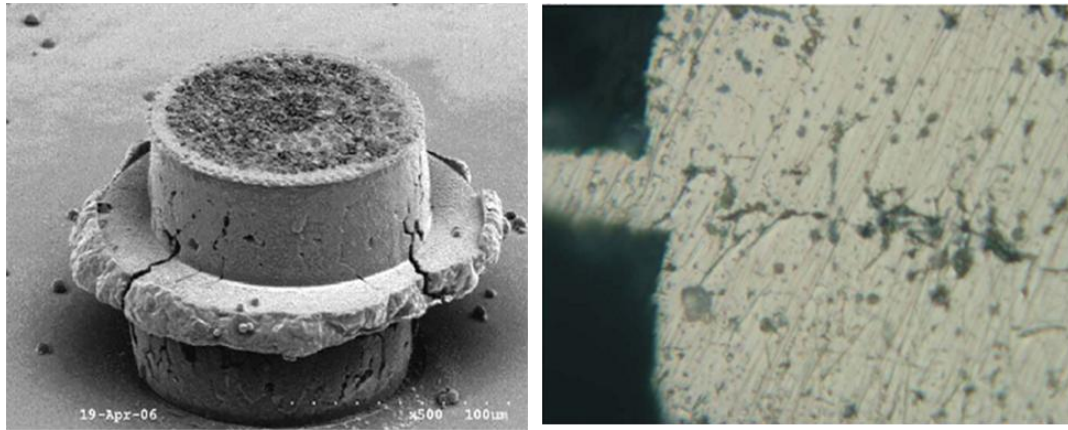


Figure 2.18: SEM image of copper pillars bonded by electroless plating and annealing

Copper Wafer Bonding

Pioneering work by Chen *et al.* discusses the result of bonding blanket copper wafer with each other at temperature range of 350-400°C followed by post-anneal treatment. Such direct bonding methods can be useful in 3D integration of IC for making vertical interconnections between chips. Blanket copper of 300nm thickness was deposited on 50nm tantalum on 4 inch Si wafers. The tantalum layer acts as the diffusion barrier layer for copper. The wafers were bonded at 400°C for 30 minutes at 4000mbar pressure and exhibited good bond properties.

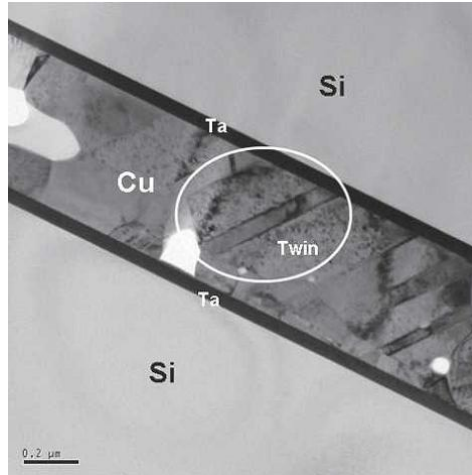


Figure 2.19: TEM morphology of bonded copper layer between silicon wafers and tantalum barrier layers

2.2.5 Emerging Alternative Bonding Techniques

This section covers bonding methods which are currently in R&D and uses techniques beyond the standard technologies described above. Such methods involve advance materials and process to realize joints between chip and substrate and have been demonstrated as proof of concept.

Solid-Liquid-InterDiffusion (SOLID)

Reflowing solder for making joints for chip-to-substrate reaches its limitation at finer pitches and maintaining barrier layer from being consumed at higher temperatures of operation becomes a challenge. Compliance of solder bumps is a critical factor for reliability in chip-to-organic substrate type packages. Such restrictions are not always applied for the case of chip-to-chip 3D interconnects where low dimensions and high interconnect density are more necessary. Thus a new interconnection technology was pioneered by Infineon Technologies to replace soft soldering by a soldering process called Solid Liquid Inter Diffusion (SOLID).

The method involves mating Cu on both sides of the chip with thin layer ($\sim 3\mu\text{m}$) of pure Sn in between them. During heat treatment, Sn melts at around 231°C and causes reaction between Cu and Sn to form intermetallic compounds (IMCs) like $\text{Cu}_6\text{Sn}_5(\eta)$ and $\text{Cu}_3\text{Sn}(\epsilon)$. This raises the melting point of the joining layer by several 100°C to T_2 as shown in Figure 2.20. The joint then solidifies isothermally at the processing temperature to complete the process. In stacking chip-to-chip, copper bumps with $3\mu\text{m}$ thick Sn layer are electroplated in wafers to form the bumps. The chip is then attached to the copper pads on another chip in two step process. First the chip is made to stick to another chip accurately using a sticking agent followed soldering. Typically the joint forms in 1 minute at 260°C in vacuum or inert gas environment. These joints need a post-anneal treatment at 300°C for 20 minutes for converting all the η phase into ϵ phase [35].

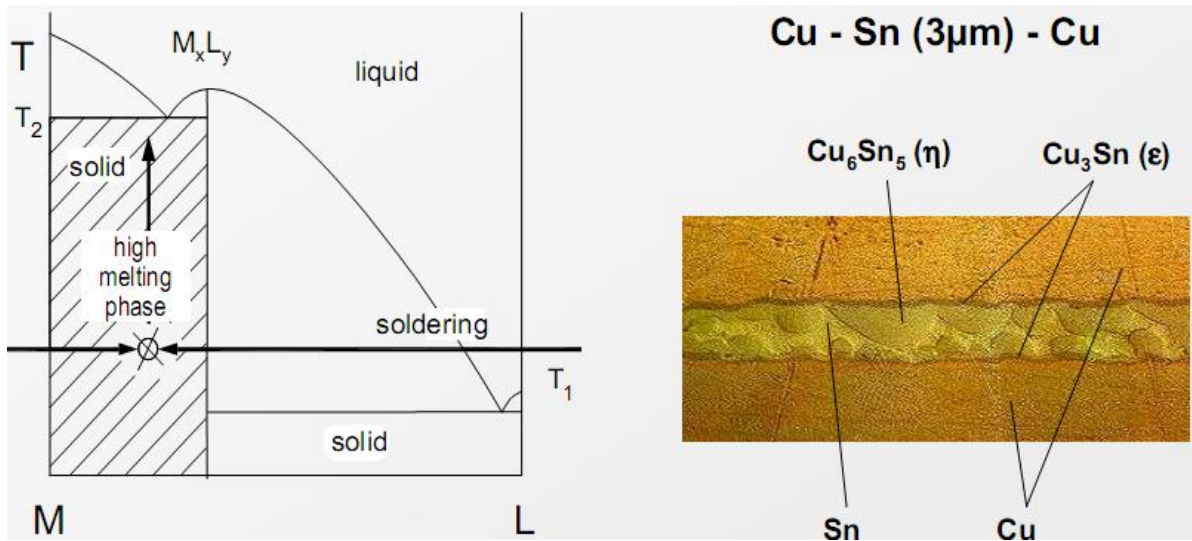


Figure 2.20: Schematic of phase diagram to explain the basics of SOLID bonding [35]

Electroless Plated Ni-B Bridge

Preferential electroless plating between the pads on the chip and substrate have been discussed earlier for forming all-copper chip-to-package interconnections. A novel

method using similar principle has been reported by Yokoshima *et al.* which uses low resistivity NiB as the bridging compound between the pads as shown in Figure 2.21.

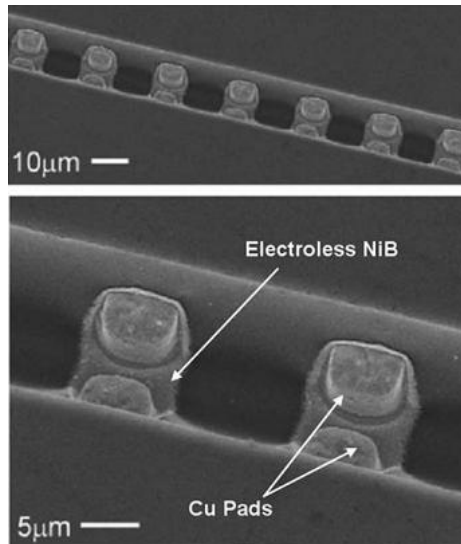


Figure 2.21: Electroless NiB bridge between Cu pads

2.3 Adhesives in Electronic Packaging

Electrically conductive adhesives were invented long back in 1950s when metal-filled thermosetting polymers were used to make electrical connection between chip and substrate [36]. Since then these adhesives have found extensive application in chip-on-glass packages for liquid crystal display (LCD) [37]. In recent years these adhesives have emerged as an important material to realize low temperature bonding for low power devices. The adhesive bonding has several advantages over solder such as:

- 1) Environment friendly solution as the joints can be Pb free
- 2) Low bonding temperature potentially reduces the thermal budget of chip attach
- 3) Capability to support fine pitch depending on the type of adhesives
- 4) Simple assembly process with no flux requirement

Essentially electrically conductive adhesives (ECAs) can be summarized as composite materials with polymer based matrix with conducting metal particles as reinforcements. Depending on the amount of fillers or reinforcements used in the adhesive, they can be classified into three broad categories – isotropic conductive adhesives (ICAs) which conduct in all directions, anisotropic conductive adhesives (ACAs) which can conduct only in Z-direction and non-conductive adhesives (NCAs) which do not have any conductive filler particles [38]. The conduction mechanisms in ICAs and ACAs can be explained based on Percolation Theory of Conduction. According to the percolation theory the resistivity of a metal filled adhesive drops drastically at a particular volume fraction of filler loading called the critical volume fraction (V_c) as shown in Figure 2.22.

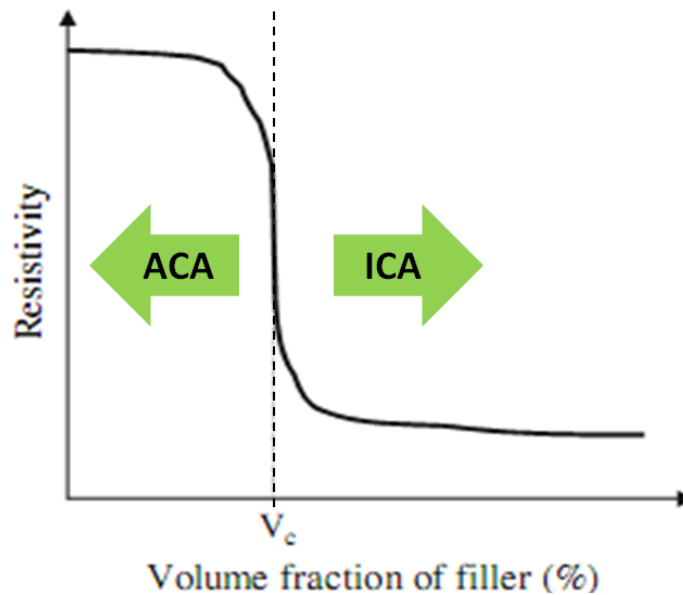


Figure 2.22: Effect of volume fraction of filler on the resistivity of adhesives

Thus ICAs are loaded with metal fillers above the critical volume fraction which enables conduction in all three directions. However in the case of ACAs, lateral conduction needs

to be eliminated, following which the filler loading is usually maintained well below the critical volume fraction.

2.3.1 Isotropic Conductive Adhesives

As mentioned earlier, ICAs have conductive filler loading beyond the threshold value to enable good conduction through them although too high filler loading avoided maintaining mechanical integrity. Typically silver flakes are used as filler in these adhesives with a loading content of about 25-30 percent. Silver is popularly used as filler because of its high thermal stability with its oxide layer compared to other fillers. The matrix can either be a thermoplastic or thermosetting resin. Most commonly used thermosetting resin is epoxy due to its superior properties while polyimide is used as thermoplastic resin.

ICAs have been used for flip-chip bonding at low temperatures [39]. ICA is printed on the back of the die using stencil or screen printing followed by flip-chip bonding to form solder like joints. The gap between the die and substrate usually needs to be filled with underfill like material. Printing of ICA for flip-chip application can become a challenge due to accuracy of pattern alignment. To overcome this problem, raised bumps or studs are fabricated on the die or substrate subsequent to which ICAs are selectively transferred to the raised surface. The finally joint resembles a flip-chip joint as shown in the Figure 2.23.

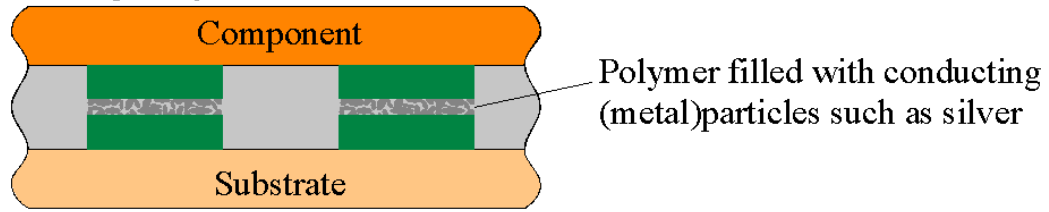


Figure 2.23: Schematic of a flip-chip joint formed by ICA

Although ICAs provide a method to form flip-chip bonding at low temperature, complex processes involved in fabricating the bumps with ICA inhibits its use in mass production. Furthermore, another polymer needs to be dispensed around the joint as underfill for better reliability similar to solder process.

2.3.2 Anisotropic Conductive Adhesive

Anisotropic conductive adhesives, in contrast to ICAs, conduct electricity only in vertical z direction. This is achieved by filler loading which is way below the percolation threshold at around 5-10 volume percent [40]. The filler particles generally 3-5 μ m in diameter can be made of pure gold, silver, nickel or even metal-coated particles with glass or polymer core. The electrical contact between the bump on die side and pads on substrate side is established by trapping of conductive particles during thermocompression bonding using ACAs as shown in Figure 2.24.

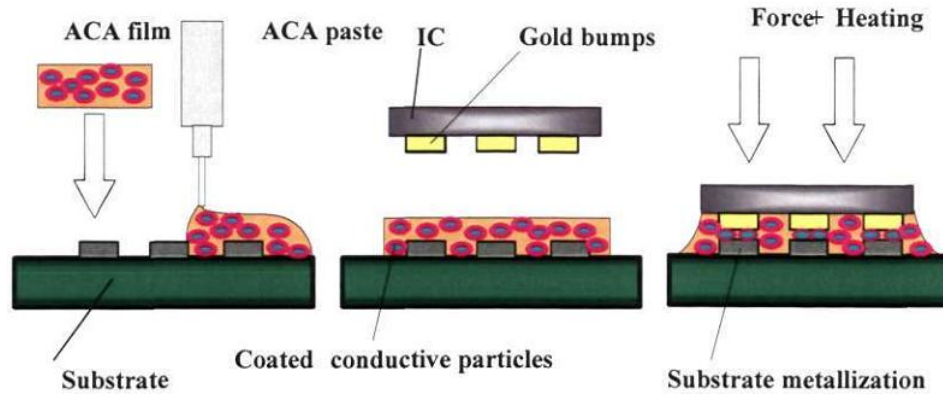


Figure 2.24: Method of forming flip-chip joint using ACAs

Low filler content in ACAs ensures no lateral conduction within the adhesive due to shorting of particles in X-Y direction. The matrix can be made of thermosetting plastic giving the joint the capability for reworkability. As mentioned earlier, ACAs have traditionally found extensive applications in LCD industry for chip-on-glass package [41]. ACA have recently emerged as an alternative to solder joints for chip-on-flex or chip-on-organic type platforms [39, 42].

The continuous downscaling of structural profiles and increase in interconnection density in flip chip packaging using ACAs has given rise to another problem. As the bump size is reduced, the current density through bump increases leading to new failure mechanisms such as interface degradation, due to inter-metallic compound (IMC) formation and adhesive swelling caused by high current stressing. This is particularly an issue in the high current carrying joint of ACA flip chip assembly where high junction temperature enhances such failure mechanisms.

2.3.3 Non-conductive Adhesives

This is another class of adhesives which do not strictly fall under conductive adhesives but function in a similar way as ECAs. These adhesives do not have conductive filler particles. Instead the electrical connection between the bump and pad is established by pressurizing the bump against the pad while the polymer or adhesive cures. The curing of adhesives, which are mostly thermosetting or B-stage epoxies, causes shrinkage in the adhesive which translates a negative pre-stress between the chip and substrate holding them together [43-44]. However, the coplanarity requirements for this type of interconnection are very strict as there are no conductive particles to fill the gaps left between contact surfaces after placement.

3. EXPERIMENTAL METHODS FOR CHIP-LAST INTERCONNECTION

This chapter describes the proposed solution for chip-last interconnection, advanced fabrication processes, assembly method developed for realizing such interconnections and techniques used for material characterization.

3.1 Copper-to-Copper Interconnection for Chip-Last Embedding

3D Systems Packaging Research Center has been pioneering a fundamental research on exploring materials for micro and nano scale interconnections with a vision to achieve ultra-fine pitch interconnections compatible with wafer based processes. The miniaturization requirements for next generation of embedded active modules dictate that the stand-off height of interconnections needs to be scaled down from 80-100 μ m to less than 20 μ m [6]. However, as the stand-off height reduces the fatigue life of the joints is affected severely which could be aggravated in the case of solders. Nano-crystalline copper was explored as a potential material for high density chip-to-package interconnections [45]. It has been shown that micro- and nano-crystalline copper have 4-10 times higher strength as compared to solders used in electronics packaging as shown in Figure 3.1. One of the methods to fabricate ultra-fine grain size copper is by electrodeposition technique in which parameters like current density and amount of additives can be used to control the grain size and structure. This method can be leveraged to develop wafer level solution for interconnections at any desired scale considering the already existing infrastructure for BEOL plating for damascene process.

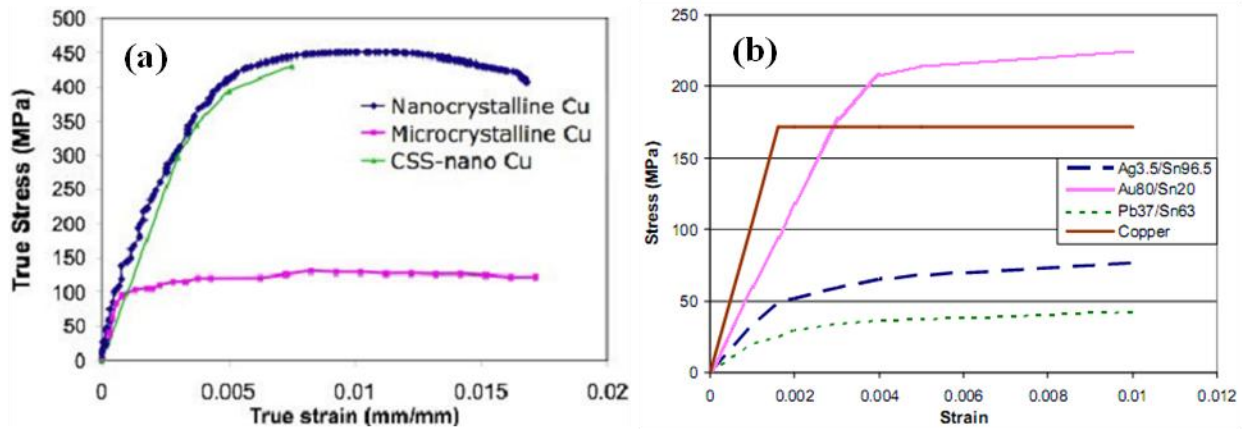


Figure 3.1: (a) True stress-strain and cyclic stress-strain (CSS) behaviour of nanocrystalline and microcrystalline copper and (b) Stress-strain curves for solders, copper and Au-Sn braze [46]

Fine grained copper has shown immense potential from electrical, mechanical and processing standpoint. The proposed solution for achieving ultra-fine interconnections includes two important aspects:

- (a) Fabrication of fine grained copper structures on both chip and package substrate at desired dimensions
- (b) Realizing copper-to-copper bonding at low temperature using advanced adhesive materials

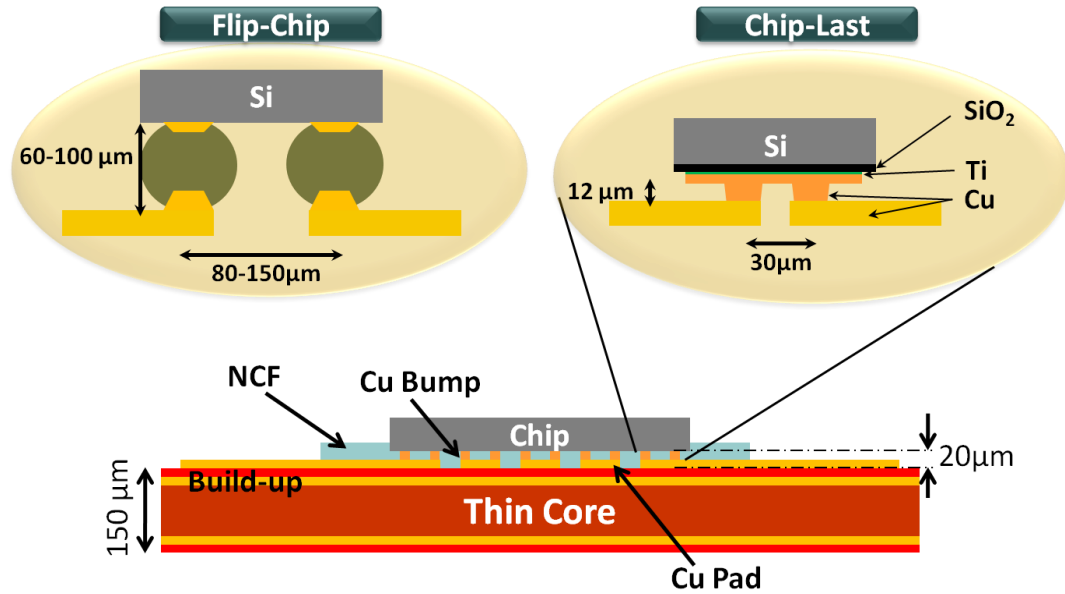


Figure 3.2: Proposed solution for chip-last interconnection

The chip-last interconnections enabling embedding of ultra-thin dies within the substrate were fabricated using electroplated copper micro bumps with a bump diameter of 15-25 μm and bump height of 12 μm . The high I/O requirements for the next generation packages need pitches below 50 μm . The copper-to-copper interconnections at 30-50 μm pitch as shown in Figure 3.2 were therefore studied in this work. Advanced thin film adhesives like nano-ACF and NCF were used for bonding the chip to the substrate at low temperature of 180°C. Thermo-compression bonding was used for attaching the chip to the substrate to yield a stand-off height of less than 20 μm . Simple low cost methods and processes were developed for enabling such chip embedding.

3.2 Fabrication Process for Micro-Copper Bumps

Through-resist plating of metals and alloys is being extensively used in modern electronics micro-fabrication processes [47]. Plating through mask has the ability to batch

process replicating structures or designs on a single wafer with least variation. This technology is emerging as an important method for bumping ICs at reduced pitches. Electroplating through patterned photoresist was explored for fabrication of copper micro bumps at 30 μ m pitch. A schematic of the baseline process for fabrication of fine grained copper micro bumps is shown in Figure 3.3. Various materials, processes and conditions used at each step of fabrication are described below. The entire process consists of forming insulation layer on Si wafer with SiO₂, seed layer using Ti and Cu, dog bone and bump layer by electroplating.

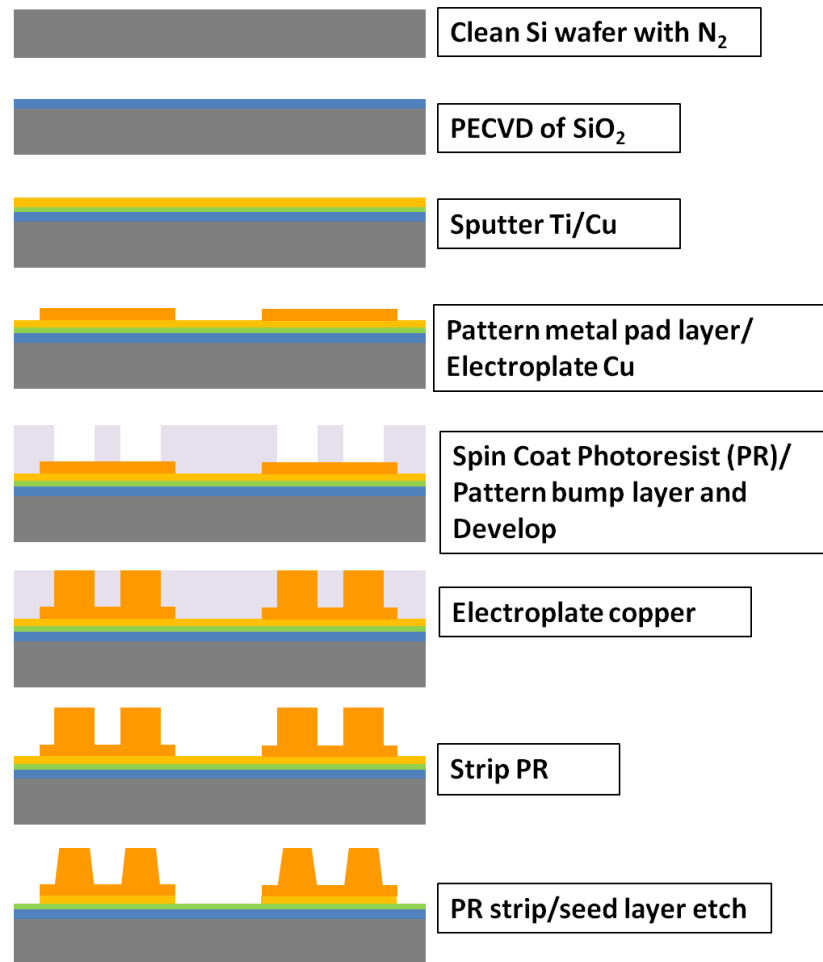


Figure 3.3: Fabrication process for electroplated copper micro bumps

3.2.1 Insulation Layer

The silicon substrate being semiconducting in nature needs a barrier layer to ensure that the conducting metal structures built on it do not have an electrical short. Silicon dioxide layer is grown on a clean silicon substrate for isolating the copper structures fabricated on it. The silicon substrate needs to be free of any dust or organic contamination prior to deposition of SiO₂ layer to ensure a uniform and good quality of film. The wafer is cleaned using standard CMOS grade wafer cleaning sequence. The wafer is cleaned in Piranha solution (solution of H₂SO₄:H₂O₂:H₂O) for 20 minutes at 120°C followed by rinse in de-ionized (DI) water. The wafer is then dipped in HF acid and quickly rinsed with DI water followed by drying with N₂ gun.

Clean wafers are immediately subjected to plasma enhanced co-vapor deposition (PECVD) for deposition of 2µm thick SiO₂ layer. A summary of conditions used on Plasma-Therm PECVD tool is given in Table 3.1.

Table 3.1: Conditions used on Plasma-Therm PECVD

Parameter	Value
Deposition Rate	500Å/minute
Time	40 minutes
SiH ₄ /N ₂ O flow rate (sccm)	100/900
Power	25W
Temperature	250°C

3.2.2 Seed Layer and Dog-Bone Layer Deposition

After insulation layer deposition, seed layer for subsequent electroplating is deposited. Titanium (Ti) and Cu are sequentially sputtered using a CVC direct current (DC) sputterer. Ti layer improves the adhesion between the copper and silicon dioxide. The thickness of sputtered Ti was 400Å and that of copper was 0.5µm. The dog-bone structures which form the pads for copper bumps are fabricated by through-resist plating. A negative photoresist is the one in which the portion of the photoresist that is exposed to light becomes insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer. Negative photo resists are known to have better adhesion properties as compared to positive ones in MEMS fabrication industry [48]. Thus, die pad fabrication was done using negative photoresist from Futurrex called NR7-1500. A bright-field mask was used for patterning the photoresist, meaning that the regions to define the die pads were dark and the surrounding regions were transparent to exposed light. The liquid photoresist was spin-coated on the wafer and baked for patterning. The photoresist processing conditions are mentioned in Table 3.2.

Table 3.2: Photoresist NR7-1500 processing conditions

Parameter	Value
Spin Speed	1) 500 RPM/500RPM ramp rate/ 5 seconds 2) 800 RPM/500RPM ramp rate/ 40 seconds
Thickness	2-2.5 μ m
Pre-bake	150°C/ 1 minute
Exposure Dose	365nm wavelength 180mJ/cm ²
Post-bake	100°C/ 1 minute

The photoresist was developed using RD6 developer for about 4-7 seconds. The developing time depends on the feature-size and the total opening area which is being developed. The wafer is then cleaned of any resist residue by descumming in an RIE tool under O₂ plasma for 2 minutes. After descum process, copper is electroplated through the resist opening to a thickness of about 2 μ m. The copper was plated at a current density of 5mA/cm² resulting in a plating rate of 450Å per minute. Details of the electroplating process chemistry will be discussed in upcoming section. The thickness of the electroplated copper was monitored using a contact profilometer. After plating the resist was removed using acetone in an ultrasonic agitator. For complete cleaning wafer is agitated in methanol followed by isopropanol with a final rinsing with DI water followed by drying using N₂ gun.

3.2.3 Bump Fabrication by Electroplating

Similar process of through-resist plating was used for plating 12 μ m thick copper bumps on the die pads. A Futurrex NR21 – 20000P negative photoresist was used for bumps due to its capability to support high aspect ratio additive plating. Futurrex photoresist is chosen because of its compatibility with various plating chemistries, and its capability to give thicker films ranging from 10-30 μ m in a single coating step. It can be stripped off with a simple liquid remover and does not need reactive ion etching like SU8 photoresist. This photoresist has a strong heat resistance and an excellent resolution capability, facilitating future down-scaling requirements. Very little or no bubbling was observed in the photoresist films which is very typical of liquid photoresists. The processing conditions for 18 μ m thick NR21-20000P photoresist are given in Table 3.3.

Table 3.3: Photoresist NR21-20000P processing conditions

Parameter	Value
Spin Speed	1) 1000 RPM/500RPM ramp rate/ 10 seconds 2) 3500 RPM/500RPM ramp rate/ 40 seconds
Thickness	18 μ m
Pre-bake	150°C/ 1 minute
Exposure Dose	365nm wavelength 720mJ/cm ²
Post-bake	80°C/ 3 minute

Precise alignment was done using Karl-Suss MA6 mask aligner using global fiducials provided on the mask. To maximize the resolution, a hard contact and high intensity light source was used. After exposure, the wafer was developed using RD6 developer for 2.5 minutes in a large plastic container using special fixtures to hold the wafer for ensuring no contact of wafer edges during agitation of developer solution. Similar to the dog bone plating process, plasma descum was performed to remove any resist residue and copper oxide layer was removed by cleaning the exposed copper surface with 10% H_2SO_4 prior to electroplating of bumps., Electroplating of copper was done at 10mA DC current for 1 hour 10 minutes. The plating thickness was intermittently monitored using a profilometer.

Copper sulfate based bath chemistry was used during electroplating. The details of the makeup of copper electrolytic plating bath are given in Table 3.4.

Table 3.4: Composition of copper electrolyte bath

Chemical	Make-up Quantity (ml)
DI water	4866
Sulfuric Acid (50% dilute)	599
Copper Sulfate	443
Copper Gleam 125 EX Carrier	61
Copper Gleam 125 EX Additive	31
	6000 ml

The bath agitation (N₂) was turned on while mixing the acid and copper sulfate in the bath to allow the tank to be cooled. The Copper Gleam 125-EX Carrier is then added and dummy plating is done at 5mA/cm² for 2 hours followed by dummy plating at 10mA/cm² for another 2 hours. Thereafter, Copper Gleam 125-EX additive is added to the bath followed by another dummy plate for at least 3 hours at 10-20 mA/cm² anode current densities. The dummy plating process ensures complete ionization of plating bath.

Table 3.5: Parameters for copper electroplating

Parameter	Value
Anode	Copper Bar
Temperature	21-29°C
Current Density	0.75-3.0 A/dm ²
Anode to Cathode Distance	20cm

The copper gleam 125-EX additive contains the active grain refiners. The copper gleam 125-EX carrier contains surface active agents that are also referred to as “wettters” or “suppressors”. Ultrasonic agitation of copper plating bath is done for reducing the porosity in the electroplating cell and for the impacting of electrolyte jets on the surface of the wafer for deposition. It can result in the limiting current density, the current efficiency, and a decrease in the concentration of polarization in acid sulfate solutions. Current density during electroplating has a large impact on the deposition rate. Insufficient current will result in poor coverage of recesses and a low general plating rate, while the presence of excessive current does not necessarily result in increased plating rate and is likely to create dull, burnt plating with impurities.

After plating, the photoresist was removed using acetone in an ultrasonic agitator. Once the photoresist was removed completely, the wafer was again cleaned with fresh acetone followed by methanol and isopropanol with a final DI rinse and drying with N₂ gun. The seed layer is then etched away starting with copper etching followed by titanium etching. The details of seed layer etching are given in Table 3.9. The etching time in seed layer removal is critical because over-etching can lead to complete removal of die pad.

Table 3.6: Etchants used for seed layer removal

Layer	Etchant	Time
Copper	H ₂ SO ₄ :H ₂ O ₂ : H ₂ O in the ratio of 1:1:15	15 seconds
Titanium	5 vol.% HF solution	5 seconds

3.3 Design and Fabrication of Test Vehicles

Test vehicles (TVs) were designed and fabricated to systematically study the reliability of the copper-to-copper adhesive interconnections with various die sizes and thicknesses. Performance of the interconnection was also evaluated by embedding the die in the organic substrate. Flip chip dies of two different thicknesses, 550µm and 55µm, along with organic substrates with or without a cavity on the surface were designed and fabricated. The schematics of cross-sections of three TVs fabricated for investigation in this work are shown in Figure 3.4.

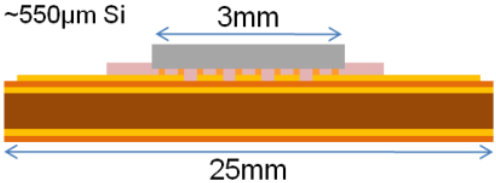
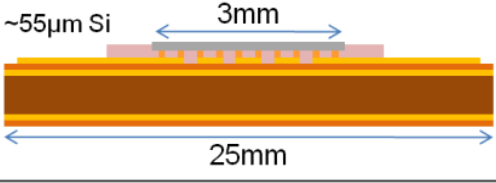
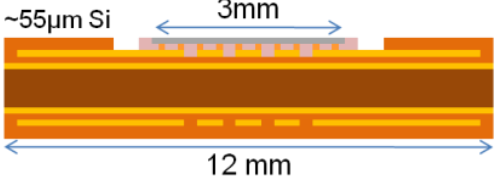
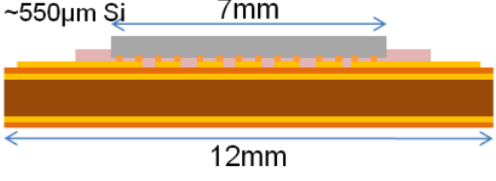
TV1 (30 μ m pitch)	
	
TV2 (50 μ m pitch)	
TV3 (50 μ m pitch)	

Figure 3.4: Schematic of cross-section of each test vehicle with critical dimensions

Each test vehicle was designed for studying specific aspects of the interconnection as enumerated in Table 3.7.

Table 3.7: Design intent for each test vehicle

Test Vehicle	Design Intent
TV1	Extract single bump resistance, daisy chain reliability
TV2	Reliability performance with embedding
TV3	Effect of high I/O and large die on reliability

3.3.1 Chip and Substrate Layout

Test Vehicle 1 (TV1)

The main objective of this test vehicle was to obtain single bump resistance and daisy chain reliability data. It consisted of a 3mm x 3mm die with 360 bumps on the periphery including 4 Kelvin test structures and 8 daisy chains with 32 bumps each. Figure 3.5 shows the position of Kelvin test structures (KP) and daisy chains (DC) in the die and substrate design. The die design also included fiducials for both alignment and orientation.

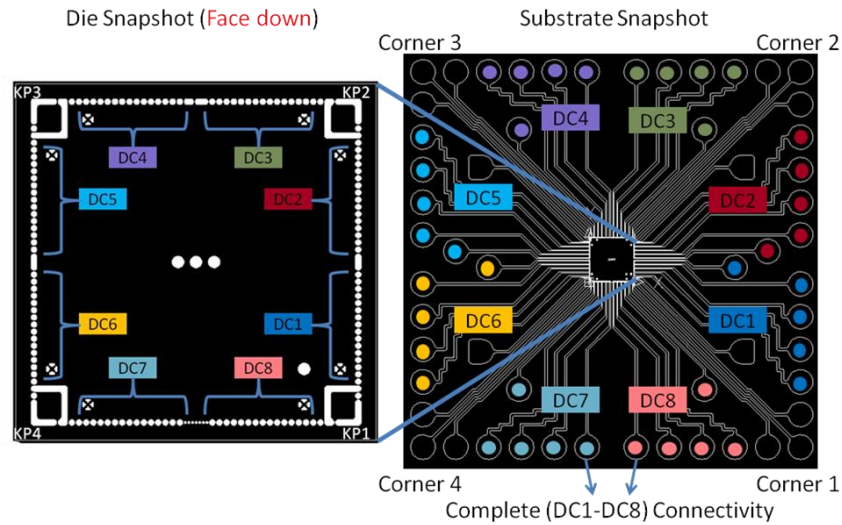


Figure 3.5: Chip and substrate layout for TV1 depicting Kelvin Probe and Daisy Chain structures

Kelvin test structures were designed to measure the single bump resistance for each of the four corner bumps since these bumps are expected to fail first. In addition, these structures were designed with a redundancy with 5 bumps built into each one of them to ensure that failure measured by Kelvin structure is indeed due to the failure of the corner-most bump as shown in Figure 3.6.

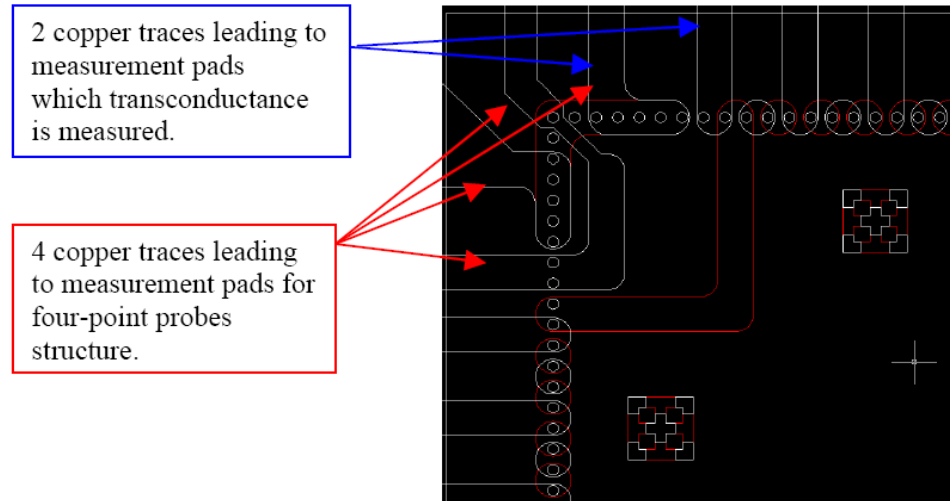


Figure 3.6: Snapshot of overlapped die (in red) and substrate (in white) design showing Kelvin Structure and Transconductance Structure

The substrate was designed for probing every eighth bump in the daisy chain. The size of the substrate was 25mm x 25mm and for TV1, it was fabricated without a cavity on the surface. Sixteen probe pads, four on each corner were dedicated to four probe measurement and forty probe pads, ten on each side were dedicated to daisy chain measurement as shown in Figure 3.5.

Test Vehicle 2 (TV2)

TV2 was designed to test the reliability of interconnect after completely embedding a thin die in an organic substrate. Die design for this test vehicle was similar to TV1. The design for TV2 was done for 3mm x 3mm dies having 216 peripheral bumps at 50 μ m pitch. As the physical tolerances for this test vehicle were more stringent as compared to TV1, the pitch was relaxed to 50 μ m. The design included 4 Kelvin test structures and 5 daisy chains as shown in the snapshot of the substrate design in Figure 3.7.

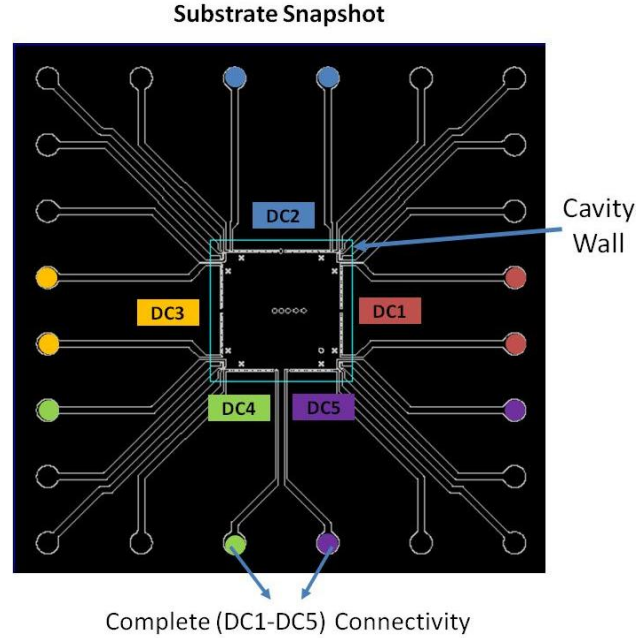


Figure 3.7: Chip and substrate layout for TV2 showing the daisy chain structures and cavity wall

The substrate was designed to facilitate probing of individual daisy chains and also the entire connected assembly. The size of the substrate was 12mm x 12mm and it was fabricated with a cavity on the surface of the substrate as shown by the cavity margin in . The clearance between the cavity wall and die edge was 400 μ m. The cavity size was determined by considering chip size as well as various tolerances such as chip size tolerances, cavity process tolerances and chip placement tolerances during assembly.

Test Vehicle 3 (TV3)

This test vehicle was designed for studying the reliability of the copper interconnects on a larger die size with high number of I/Os including peripheral and area array bumps. Die size of 7mm x 7mm was used for this test vehicle. The die design included 537 bumps at 50 μ m pitch arranged around the periphery of the die. A square grid of 10 x 10 bumps at 200 μ m pitch was also incorporated at the center of the die. The design consisted 5 daisy

chains along the edges of the die. The substrate was designed to probe individual daisy chains as well as the array of bumps in the center. The size of the substrate was 12mm x 12mm. The design enabled probing of peripheral daisy chains and the entire array of center bumps as shown in the snapshot of substrate design in Figure 3.8.

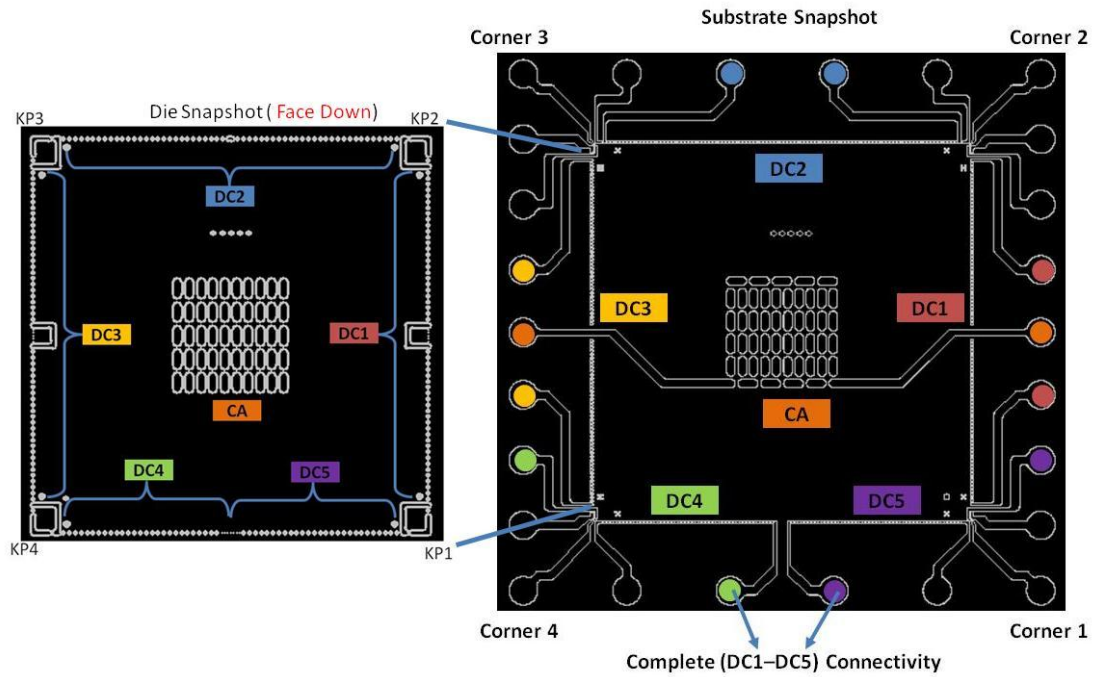


Figure 3.8: Bump layout and substrate routing design

3.3.2 Fabrication of Dies with Copper Bumps

Die fabrication was done on 4 inch silicon wafers. The die pads and copper bumps were fabricated on the bare silicon wafers by semi-additive plating of copper as described in detail earlier. A summary of critical dimensions used in die fabrication process is given in Table 3.8.

Table 3.8: Details of dies fabricated for TV

Die Size	3x3mm²/ 7x7mm²
Die Thickness	550μm and 55μm
Bump Height	12-13μm
Bump Pitch	30-50μm
Bump Diameter	15-25μm

with the wafers used for fabrication were 550μm in thickness. For thinner dies, the wafers were thinned down to 55μm thickness by back grinding done at Disco Corporation. In order to improve the ductility of copper electrodeposits, it is important that the copper is annealed to increase the grain size of copper [49]. The wafers were annealed in a N₂ environment at 125°C for 1 hour. The copper structures on the wafer were given a surface finish to avoid oxidation of copper using Electroless Nickel and Immersion Gold (ENIG) discussed in the later section. The wafers were then diced according to die size.

3.3.3 Fabrication of Build-up Substrate with Cavity

As bump pitch for embedded die was targeted to be three times less than the standard flip chip packages, a new high wiring-density build-up substrate was required. Therefore, the substrate fabrication for all the test vehicles was done using a new organic build-up substrate developed for such fine-pitch applications.. The substrate consisted of a low dielectric constant ultra-thin build-up film laminated to a low loss thin core [50]. RXP-1 (Rogers Corp. ©) was used as core material and RXP-4 (Rogers Corp. ©) was used as

build-up adhesive material [51]. The key properties for both the materials have been listed in Table 3.9.

Table 3.9: Material Properties for core and build-up material

Property	RXP-1 (Core Material)	RXP-4 (Build-Up Material)
CTE – X/Y (0-100°C)	13-14	60
CTE – Z (25-100°C)	41-43	68
Tensile Modulus (MPa)	9700	1613
T _g	>300	178

The bondpads and fine line routing of 8µm thickness on the build-up substrate was done using semi-additive plating process. Dry film photoresists from DuPont™ were used for patterning the substrates. A process flow for metallization of build-up substrate has been shown in Figure 3.9.

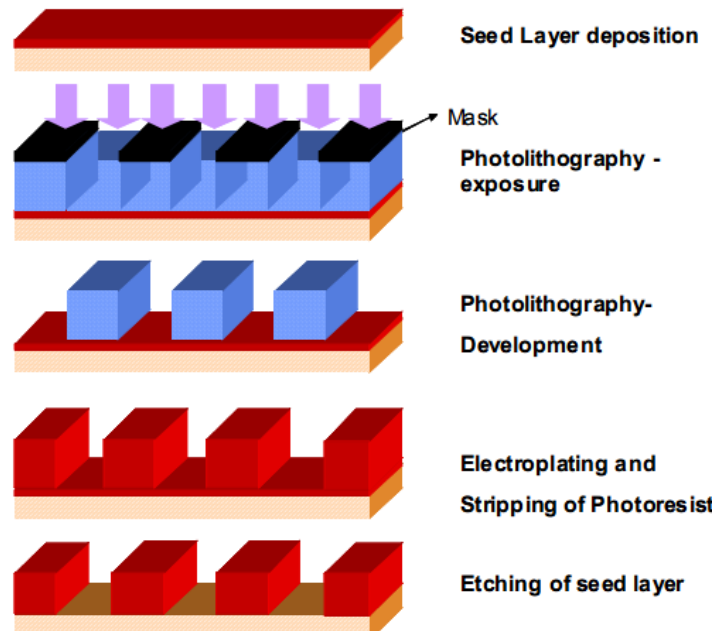


Figure 3.9: Semi-additive metallization on build-up dielectric [52]

For embedding the dies, a cavity of 60µm thickness was fabricated on the surface of the substrate as shown in Figure 3.10. The exposed metal pads were cleaned of any debris due to laser ablation using a plasma treatment. $\text{CF}_4/\text{O}_2/\text{N}_2$ plasma was used at 100°C for 5 minutes for complete cleaning of metal pads.

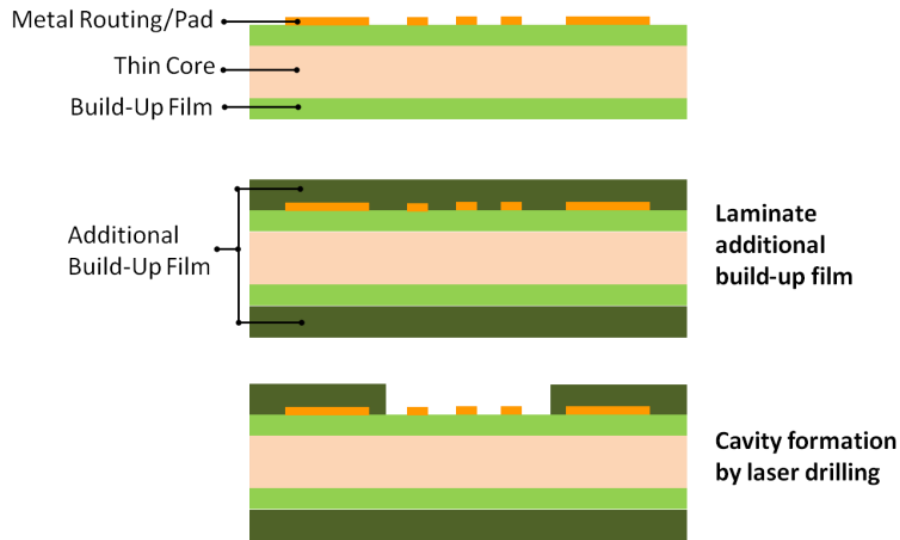


Figure 3.10: Schematic showing process steps to fabricate cavity on the substrate

3.3.4 Surface Finish using ENIG Process

Electroless Nickel and Immersion Gold (ENIG) is a type of electroless plating process which is extensively used in electronics industry for giving surface finish on the copper traces and bond pads on the PWB. It consists of NiSO_4 based chemistry for electroless plating of Ni followed by a thin layer of immersion gold based on gold cyanide chemistry for protecting the nickel from oxidation. ENIG chemistry offers much strength including excellent wettability, conformality, surface oxidation resistance and long shelf-life.

The test vehicles were given a surface finish using Aurotech chemistry and process developed by AtotechTM. The Aurotech process deposits uniform electroless nickel/gold coatings over exposed copper surfaces as well as in plated through-holes, even those with

high aspect ratios. Aurotech is particularly well suited to provide perfect corrosion resistance for ultra fine line circuitry by optimum coverage of edges and sidewalls [53].

The ENIG process consisting of pre-clean, microetch, activation, electroless nickel and immersion gold was carried out in the prescribed sequence. As a pre-treatment process before performing electroless nickel plating, the Cu metal was cleaned by a series of chemicals. Failure to remove unwanted contaminants from the surface would result in poor adhesion of nickel, and thus poor plating. Each pre-treatment chemical was followed by water rinsing to remove the chemical that adheres to the surface. The main steps used in ENIG are described below.

Step 1: Organic Debris Cleaning

The first step consists of degreasing to remove organic contaminants from the metal surface. It prepares the copper surface for the subsequent microetching.

Step 2: Microetching / Oxide Cleaning

Microetching removes the oxide layer from copper, providing a pristine copper surface. It gives an optimum roughness of the copper surface to get an excellent adhesion of the electroless nickel. However, microetching chemistries based on peroxide could be too aggressive on fine line circuitry. Instead, 5vol. % sulphuric acid solution was used dissolve oxides from the copper surface.

Step 3: Pd poisoning

Copper structures on the substrates are plated on a thin electroless plated copper layer. The dielectric surface is often activated for electroless copper plating using palladium. Pd poisoning step is included to remove any residual Pd on exposed dielectric surfaces to

ensure that the exposed dielectric surfaces do not interfere in Ni and Au deposition by shorting copper structures.

Step 4: Aurodip

Aurodip is a organic based solution provided by Atotech which used to condition the surface before activation.

Step 5: Predip / Oxide Cleaning

The pre-dip is the final step to condition the surface before activation. The copper surface was cleaned of any oxides that may have developed due to previous cleaning and rinsing steps. The pre-dip was made up of 5vol. % sulphuric acid solution.

Step 6: Activation

The activator dip creates a thin uniform layer on any copper surface exposed to the solution. A palladium sulphate based activator was used, with a palladium concentration of $50 \text{ ppm} \pm 10$. A thin layer of palladium was created by an ion exchange reaction between copper and palladium.

Step 7: Electroless Nickel

Electroless nickel plating is an auto-catalytic process used to deposit a coating of nickel on the palladium catalyzed copper surface. The nickel phosphorous coating is amorphous therefore provides excellent corrosion resistance. Deposition speed and phosphorous content of the nickel solution was kept constant via temperature and pH-control. The pH was kept between 4.8 and 5.3 and the temperature variation was within $85^{\circ}\text{C} \pm 5^{\circ}\text{C}$. With a nickel concentration between 5.7 and 6.3 g/L, the nickel deposition rate achieved was about 0.18 to 0.25 $\mu\text{m}/\text{min}$.

Step 8: Immersion Gold

The immersion gold is an exchange reaction between the nickel layer and the gold bath: two gold atoms displace one nickel atom. The gold applies itself to the nickel plated areas. The immersion gold bath plates fine dense gold deposit of 0.13 μ m maximum thickness at a temperature range of 70°C to 90°C. For this work, the bath was kept at 85°C. The bath was kept at a constant pH of 4.8. To adjust the pH, a 5N KOH solution or a 5% sulfuric acid solution were used, depending on the bath being too acid or too basic. The dissolution of nickel into gold bath does not interfere with the deposition quality. Optimization of plating time for activation, nickel plating and gold plating was done for coating Ni/Au on silicon dies and organic substrates.

3.3.5 Assembly Process for 30 μ m Pitch Copper Interconnections

Assembly process using adhesive bonding becomes challenging at fine pitches as alignment tolerance shrinks significantly. The visibility of fiducials through the NCF layer adds to the already stringent alignment requirements. Early studies for optimizing the assembly process have been reported where a glass substrate was selected for enabling back side inspection of alignment [54]. Visibility of NCF depends on the amount of non-conductive filler in the epoxy matrix. Thus NCF used in this work was void of any filler. The assembly was done using FINETECH Fineplacer© Lambda assembly tool with an alignment accuracy of $\pm 1\mu$ m. Tilt of the die while placement on the substrate was addressed by using a tool head with gimble which allowed for both pre-leveling and automatic leveling during assembly.

The assembly process for chips bonded on the surface of the organic substrate and within a cavity of the organic substrate was identical as shown in the schematic in Figure 3.11. NCF was pre-bonded to the organic substrate at 90°C for 15 seconds followed by

cooling to room temperature and removal of NCF liner. The size of NCF bonded in the cavity of the organic substrate was contained within the cavity to avoid overflow of NCF over the cavity wall. The die was aligned to the substrate and placed on it after pre-heating it to 85°C to reduce the viscosity of the NCF. The die and the substrate were subjected to a pre-determined load and cured at 180°C for 30 seconds. The applied load for 3x3 mm² die size was 21N load which translates to a contact pressure of ~300MPa on the surface of the bumps. The applied load for 7x7 mm² die size was calculated based on the effective surface area of all the bumps so that the contact pressure was still maintained around ~300MPa.

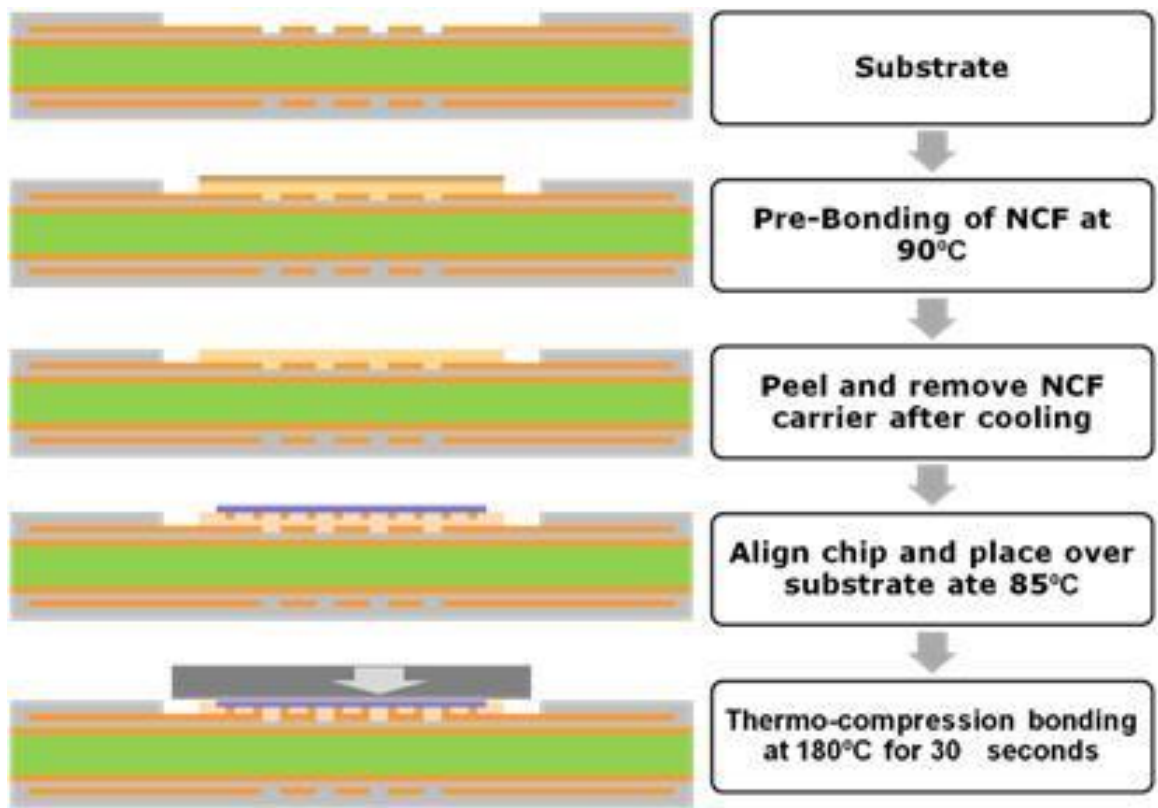


Figure 3.11: Assembly process flow for die embedding using adhesive bonding

3.4 Thermo-Mechanical Reliability Testing

Copper-to-copper interconnections using adhesive bonding was studied for reliability under high temperature and humidity conditions by U-HAST and HTS test. These tests were selected to study the compatibility of adhesive interconnections on organic build-up substrate as compared to glass or silicon substrate reported previously [54]. Sample-size for each of these variations was ~8-10 samples per test. In order to maintain consistency with the standard reliability testing procedure in the industry, all the samples were subjected to a pre-conditioning (pre-con) as per joint IPC/JEDEC Standard J-STD-020A before subjecting to any reliability tests. It involves baking the assemblies at 125°C for 24 hours prior to subjecting them to moisture sensitivity level-3(MSL-3) at 60°C and 60% RH for 40 hours followed by 3 times reflow with peak reflow temperature of 260°C. For HTS test, the assemblies were subjected to 175°C in air for 72 hours in accordance with JEDEC standard JESD22-A103C (condition C). Similarly, for HAST, the testing involved subjecting the assemblies to 130°C and 85% relative humidity (RH) for 96 hours as per JEDEC standard JESD22-A118 (condition A).

The mechanical integrity of the copper-to-copper adhesive joint was studied using thermal shock testing. All the test vehicles (TV1, TV2, and TV3) were tested under TST as describes in JEDEC standard JESD22-A104C (condition B). Assembled samples were subjected to a cyclic thermal loading in air from -55°C to 125°C with a dwell time of 15 minutes at each extreme temperature.

3.5 Characterization of Adhesive Bonded Copper-to-Copper Joints

Joints formed by direct copper-to-copper bonding using adhesives were characterized for studying the morphology of electroplated copper, correlation of mechanical property with

grain structure of copper and understanding the bump-pad interaction during low temperature bonding by studying the diffusion across the interface. Advanced material characterization techniques used in the process of study have been listed below.

3.5.1 Field Emission Scanning Electron Microscopy

The morphology of copper grain structure and failure analysis of interconnections were studied by observing the cross-section of bump-pad interfaces using Thermally Assisted Field Emission Scanning Electron Microscope (FESEM LEO 1530 and Hitachi 3500H). These tools have a capability to resolve 3 nm feature size at a low voltage of 1 kV.

3.5.2 Energy Dispersive X-Ray Spectroscopy

Diffusion of Copper, Nickel and Gold across the interface was studied using EDS. Line scans across the interface and area scan for individual elements were used to study the distribution of each element across the bump-pad interface.

3.5.3 Cross-section Preparation using Ion Polishing

Ion beam polishing of cross sectional samples for SEM imaging studies of grain structure produces a flat mirror-finish often not achievable by mechanical polishing. This technique was used to remove smeared copper on the cross-section samples which could interfere in the microstructural evolution of the copper bumps.

3.5.5 Four-Point Probe Measurement

Single bump contact resistance was measured using four-point probe technique on Kelvin Test Structures. The four-point probe setup included Keithley 2400 Source Meter and four fine tip probes. Current (I) in the range of 0.02-0.1Ampere was passed through the test structures and voltage (V) drop across the bump was measured. Resistance was calculated as the slope of the obtained V/I curve.

4. RESULTS AND DISCUSSION

This chapter discusses the results of fabrication of micro-copper bumped test vehicles for studying the reliability performance of adhesive bonding at 30 μ m pitch. The chapter begins with results of developing defect free micro-copper bumps with high coplanarity followed by the results and discussion for assembly process development for all the three test vehicles including embedding of 55 μ m thin silicon dies using copper-to-copper interconnections. The section concludes with extensive discussion on reliability test results obtained from each test vehicle and failure mode analysis for adhesively bonded joints using NCF.

4.1 Fabrication of Coplanar Copper Bumps

One of the challenges for fabricating electroplated copper bumps 15 μ m in diameter and 13 μ m in height is to have defect free bumps. Several parameters influence the surface quality and geometry of the bumps at such dimensions. The photoresist process and electroplating of copper are two such processes that play a critical role in controlling the defects induced during bump fabrication.

4.1.1 Effect of Lithography and Electroplating on Bump Geometry

Processing of thick photoresist leads to a risk of cracking during baking. Such photoresist cracking can be induced due to several reasons. The most common reason being the flaws induced during spin-coating of photoresist. In order to avoid these flaws, it is imperative to have a completely clean wafer surface void of any contaminant particles. Photoresist should also be allowed to cool down slowly after post exposure baking to ensure sudden thermal shock does not crack the brittle photoresist. Like any other photoresist

processing, the developing time is critical to attaining precise patterns with vertical side walls. Under developed photoresists can lead to unexposed metal surface while over developed photoresists can have severe under-cut [55]. Because the bumps were to be fabricated at ultra-fine pitch, the tolerance for over developed photoresist was extremely tight. Figure 4.1 shows the effect of under-developed photoresist on the final geometry of copper bumps. Because the progress of photoresist development is monitored through optical examination of the openings, the extent of development becomes difficult to ascertain. Hence, optimization of photoresist development time for specific thickness needed to be done.

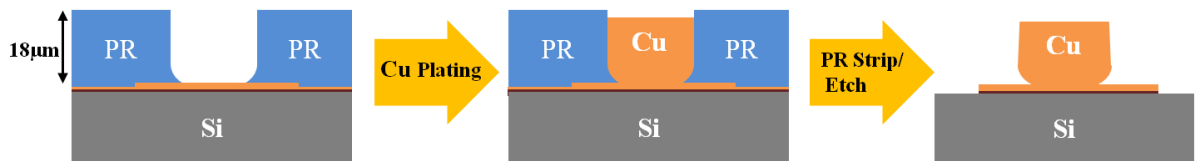


Figure 4.1: Under developed photoresist (PR) leading to defective bumps

The electroplating through under-developed photoresists can lead to tapering at the base of the bumps and unwanted voids at the surface of the bumps as shown in the SEM image of the defective copper bumps in Figure 4.2.

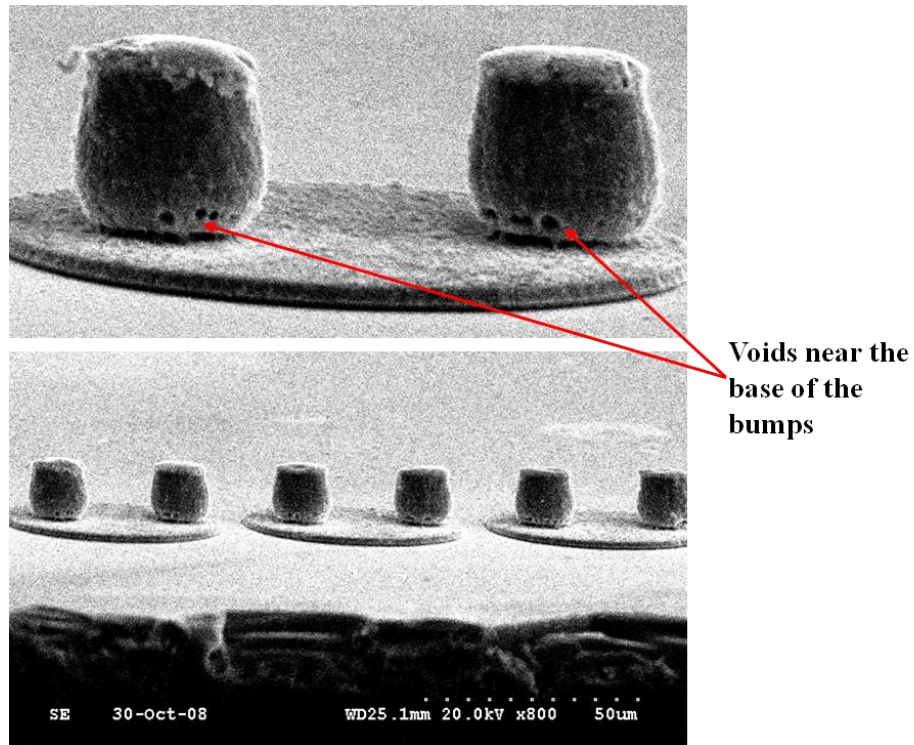


Figure 4.2: SEM image of defective copper bumps

Overplating is another cause of defective bumps leading to mushrooming of bump's top surface as shown in Figure 4.3. Non-uniform plating across the surface of wafer leads to such defects in bumps. The mushrooming at the head of bump occurs due to electroplating of copper uniformly in all three directions above the surface of photoresist.

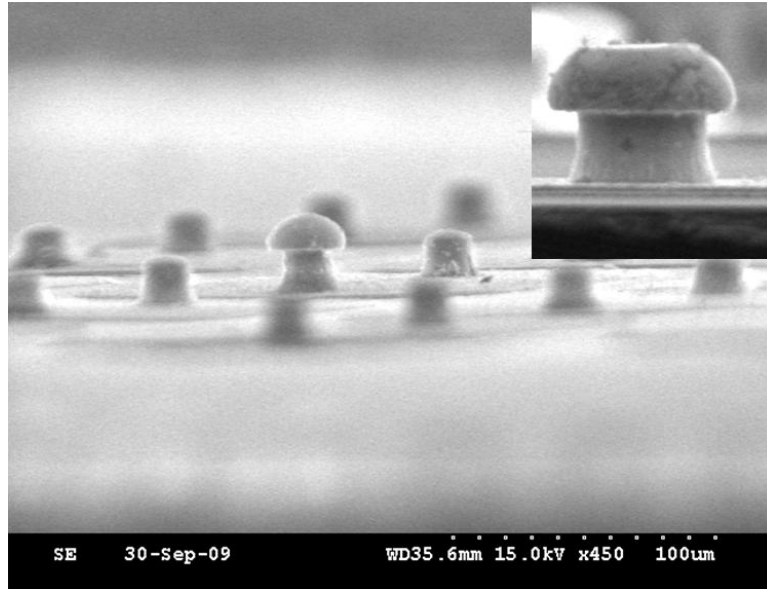


Figure 4.3: Overplated copper bumps leading to mushrooming

Optimum current density of $0.2\text{--}1\text{ A/dm}^2$ with aggressive bath agitation was needed to ensure a uniform plating of copper through the photoresist. In order to ensure no tapering occurs at the base of the bump, the resist was slightly over developed and plasma cleaned to ensure clean exposed copper surface for electroplating. Copper bumps of $13\mu\text{m}$ height and $15\mu\text{m}$ diameter were successfully fabricated on silicon die at $30\mu\text{m}$ pitch as shown in Figure 4.4.

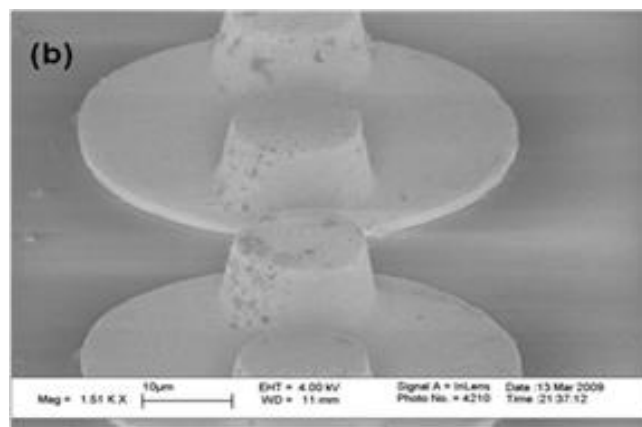


Figure 4.4: Electroplated micro-copper bumps on silicon at $30\mu\text{m}$ pitch

4.1.2 Coplanarity Study of Micro-Copper Bumps

Another challenge for successful assembly using conductive adhesives is to have uniform bump coplanarity [56]. In case of traditional ACA like adhesives, the entrapped fillers deform to adjust to the non-uniformity in bump height across the die leading to successful electrical connection in all the bumps. However, in case on non-conductive adhesives where electrical connections is not dependant on micron size filler particles, the bump uniformity requirement becomes even more stringent. The Cu plating process was optimized to yield highly coplanar copper bumps as shown in the Figure 4.5.

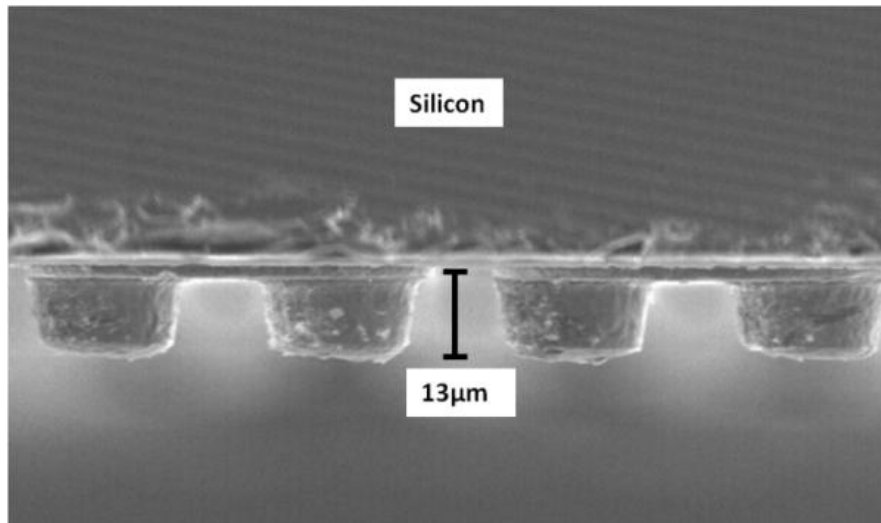


Figure 4.5: SEM image of highly coplanar copper bumps after process optimization
Die bump coplanarity was evaluated using three randomly selected dies from the same wafer and 38 readings were taken at random positions including all four edges of the die. The result of the study is shown in Figure 4.6. The measured total height (including the pads on the die side) for most of the copper bumps was found to be 13.1µm with a standard deviation of 0.45µm. All the bumps had a height within 2 standard deviations.

With a total variation of $\pm 1\mu\text{m}$ in bump height it was expected that with a minimum deformation of $1\mu\text{m}$ during assembly would ensure that every bump-pad contact is made.

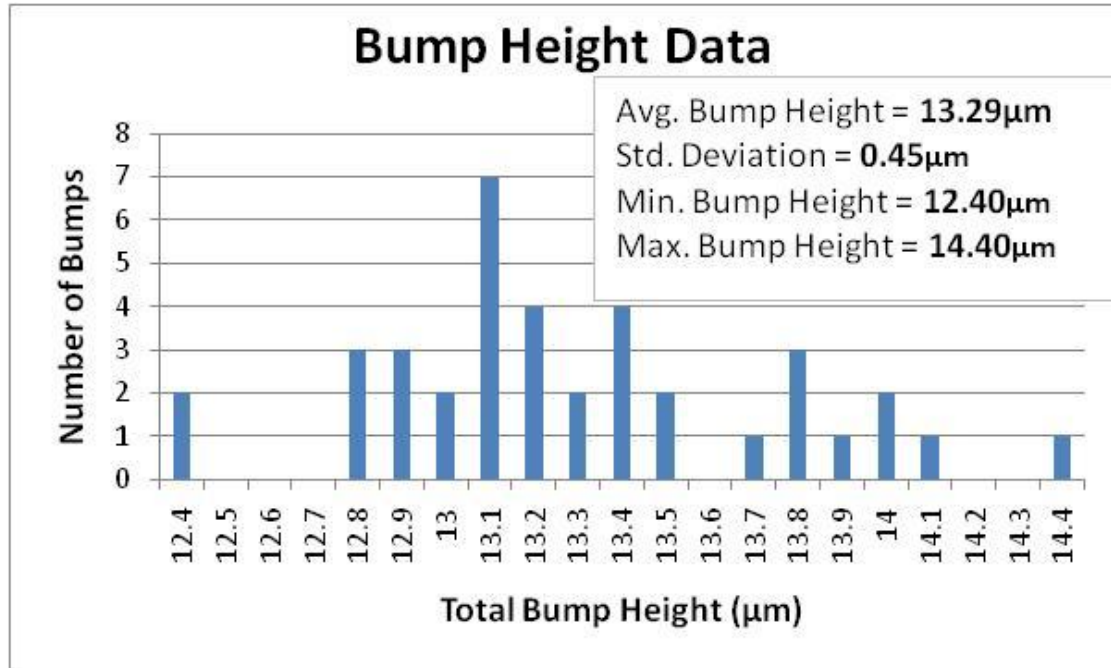


Figure 4.6: Bump height data for 38 bumps collected randomly from different parts of the wafer

4.2 Enhancement of Copper-to-Copper Electrical Contact

Pure copper thin films have been extensively studied for oxidation kinetics and have been shown to oxidize readily below 200°C in air [57]. This creates a problem for a forming direct copper-to-copper joint for electrical conduction as surface of copper bumps and pads oxidize readily during bonding process. As copper oxide is a poor conductor of electricity, even thin film of copper oxide between the bump and pad can cause electrical open or poor joint properties. To enhance the performance of joint and ensure low contact resistance, inert surface finish for copper structures was explored. ENIG was chosen as the surface finish for copper bumps and pads due to its high conformality and

excellent oxidation resistance. The steps for cleaning and plating of ENIG were described in the previous chapter. As the goal of doing ENIG surface finish was to prohibit oxidation of copper during bonding and the tolerance between the closest bump pads was $10\mu\text{m}$, the thickness of Ni was targeted to be 500nm and Au to be less than 100nm . The plating rate of electroless Ni on copper bumps is very high; therefore, precise control over plating time is needed to yield the required thickness. Nickel plating rate was calculated by measuring the thickness of Ni plated on a blanket copper substrate for 15 minutes as shown in Figure 4.7.

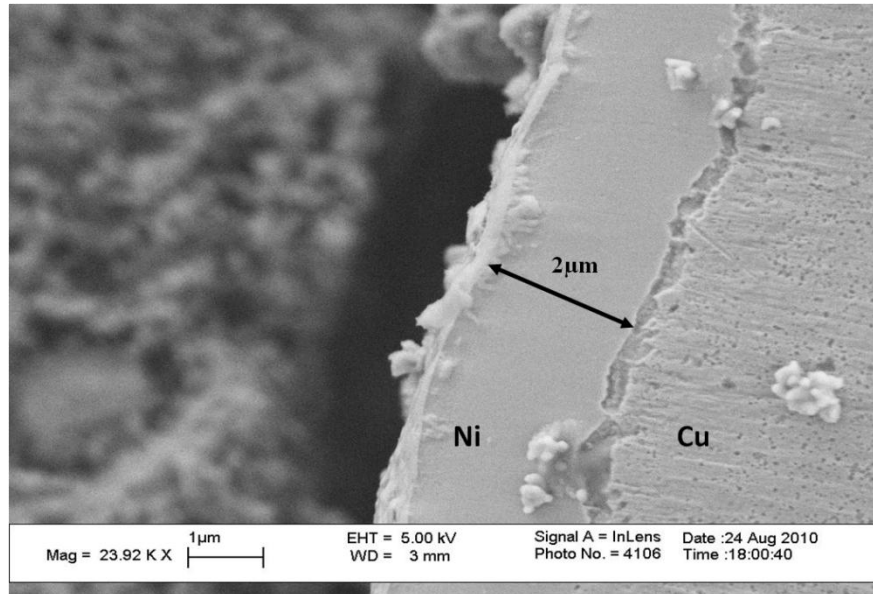


Figure 4.7: SEM image of electroless Ni plated on Cu Substrate for 15 minutes

Both die and substrate were given a surface finish using ENIG. Because of the ultra-fine pitch bumps, the spacing between the adjacent bump pads was $10\mu\text{m}$, requiring extensive optimization to ensure a good quality surface without shorting the pads. A series of experimental steps were performed to optimize time for activation and plating of nickel and gold. A sequence of each step performed in the ENIG process along with bath

composition, plating time and process temperature has been mentioned in **Table 4.1**. The optimized time required for activation was found to be 2 minutes. In addition, as mentioned earlier, the organic substrates needed a Pd poison step to ensure that the build-up surface does not get activated for ENIG. The effect of time optimization for activation on ENIG coated copper pads is shown in Figure 4.8.

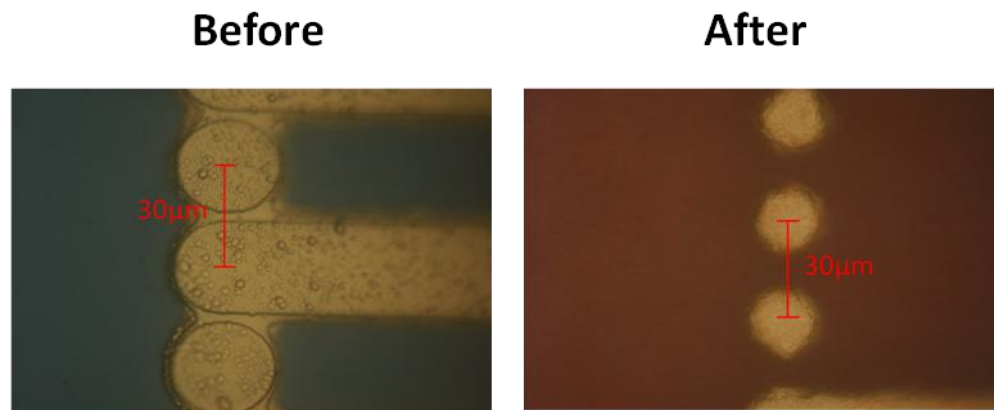


Figure 4.8: Copper pads with ENIG after process optimization

Table 4.1: Details for ENIG process: bath composition, temperature and time

Oxide cleaning	H ₂ O	950 mL	RT*	30 s
	H ₂ SO ₄	50 mL		
Pd Poison	H ₂ O	225 mL	40°C	5 min.
	Proactive DP	250 mL		
	H ₂ SO ₄	25 mL		
Cu cleaning	H ₂ O	375 mL	45°C	5 min.
	H ₂ SO ₄	33 mL		
	SF Acid	100 mL		
Rinse	Rinse: Water beaker			
	Rinse: Spray			
Oxide cleaning	H ₂ O	950 mL	RT*	30 s.
	H ₂ SO ₄	50 mL		
Rinse				
Aurodip	H ₂ O	870 mL	70°C	2 min.
	Aurodip	130 mL		
Rinse				
Predip / Oxide cleaning			RT	1 min.
Activator	H ₂ O	750 mL	RT	Variable
	H ₂ SO ₄	50 mL		
	Activator	200 mL		
Rinse				
Electroless Ni	H ₂ O	390 mL	85°C	Variable
	Make up	75 mL		
	Part A	30 mL		
	NH ₄ OH	10 mL		
Rinse				
Immersion Au	H ₂ O	700 mL	85°C	Variable
	SF Plus	238 mL		
	SF Starter	1 mL		
	KAuCN	3 g		
	H ₂ SO ₄ / KOH	pH = 4.8		
Rinse	Water beaker + Hot water beaker			

4.3 Thermo-Compression Assembly for Adhesive Bonding

Fundamental concepts about electrical contacts made between metal surfaces using non-conductive adhesives have been reported by Kristiansen *et al.* Two most important parameters involved in realizing electrical connections between metal surfaces in such adhesive bonding are: (1) load applied on the die and (2) bonding temperature. Chung *et al.* have discussed the method of forming gold-to-copper joints using NCF where heat,

pressure and time of bonding are shown to be critical factors in achieving good connections as shown in Figure 4.9 [58].

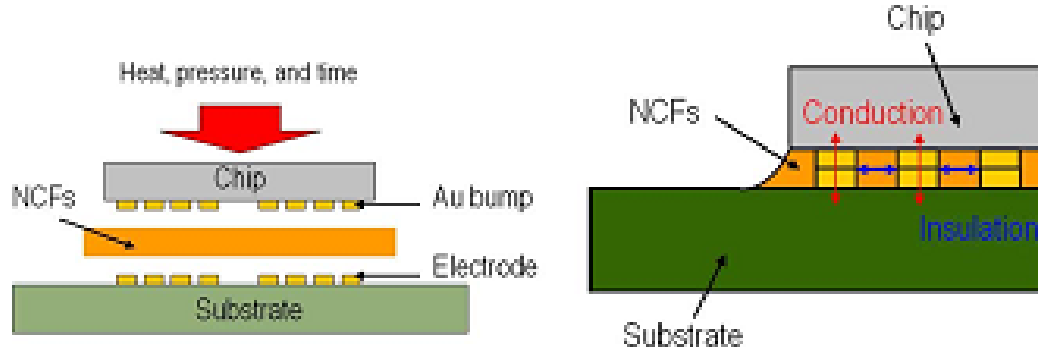


Figure 4.9: Schematic of bonding process using NCF for Flip-chip on Board (FCOB)

4.3.1 Material Characterization of Adhesive

The NCF material was characterized using Dynamic Mechanical Analysis (DMA), Thermo-Mechanical Analysis (TMA) technique and Differential Scanning Calorimetry (DSC) for material properties like coefficient of thermal expansion, glass transition temperature, curing temperature and storage modulus of the adhesive polymer [59]. The glass transition temperature (T_g) of cured NCF was found to be around 115°C based on the storage modulus and loss modulus curves shown in Figure 4.10. The results also show that the storage modulus of cured NCF is approximately 2GPa at room temperature.

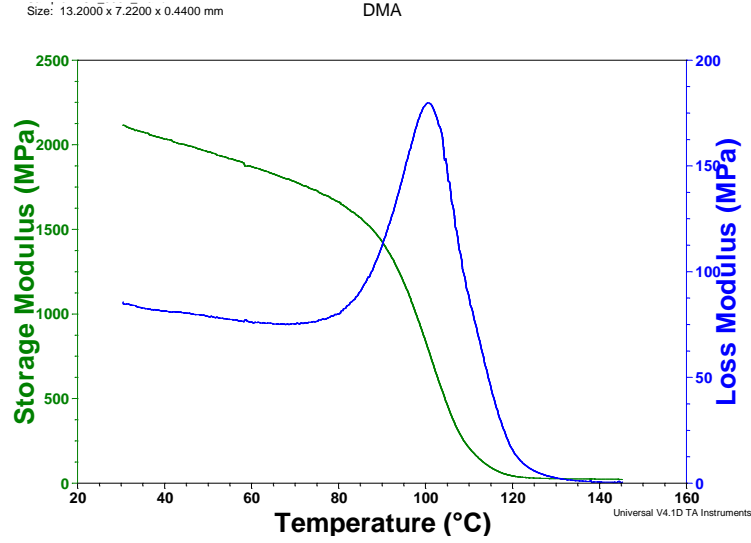


Figure 4.10: Results of DMA for NCF without silica filler

The CTE of NCF was measured using TMA as shown in Figure 4.11. The CTE, calculated as the slope of tangents to the curve before and after T_g was found to be 64ppm/°C before glass transition temperature and 193ppm/°C after it.

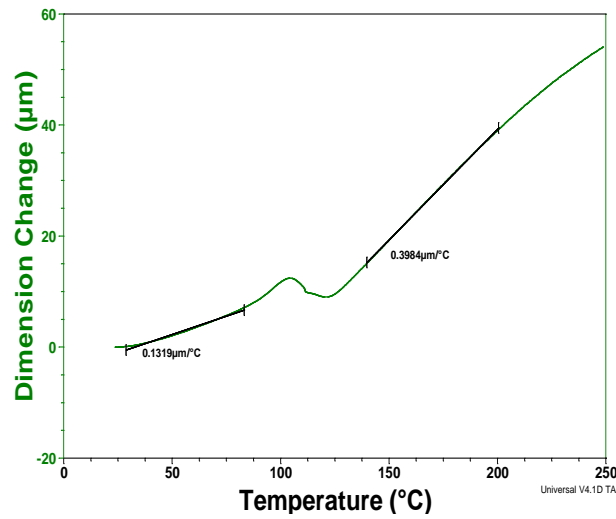


Figure 4.11: Result of TMA done on NCF without silica filler

As mentioned earlier, the bonding temperature of NCF based assemblies depends on the curing time and temperature for the epoxy resin which forms the bulk of the NCF material [60]. The curing temperature of the adhesive can be ascertained using heat

flow curve obtained from DSC technique. Figure 4.12 shows the results of a typical heat flow curve obtained for NCF material used in this study. The result shows that the resin underwent isothermal cure around 117°C leading to extensive cross-linking of monomers used in the resin to form a highly cross-linked rigid polymer.

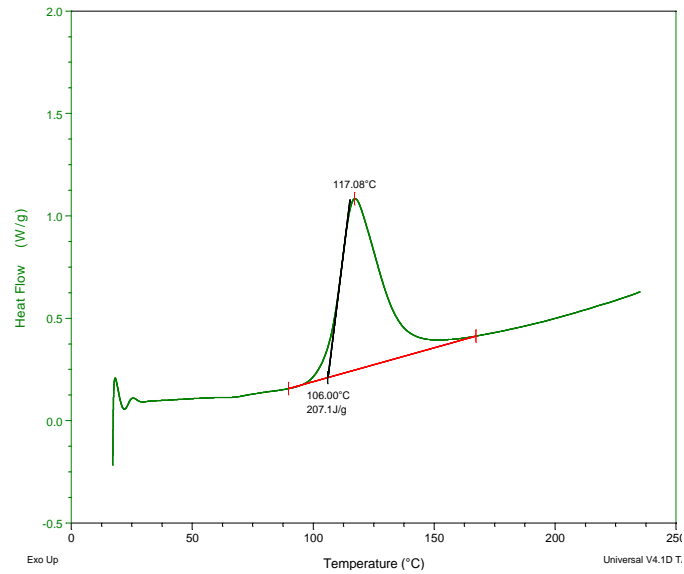


Figure 4.12: Result of DSC analysis performed on the NCF resin

The properties of the NCF used for copper-to-copper bonding have been summarized in Table 4.2.

Table 4.2: Measured properties of the NCF

Property	Value
Storage Modulus	2GPa
Tg	~115°C
CTE	65-70 ppm/°C

4.3.2 Thermal Profile for Bonding

Based on the characterization results of the NCF, thermo-compression bonding profile was developed. Extent of curing of NCF can be controlled using the time and peak temperature of bonding. The curing process involves gaseous release of residual solvents used for formulating the NCF resin. The bonding was done at 180°C for 300 seconds as shown in Figure 4.13 to ensure complete curing of NCF although the NCF cures in less than 30 seconds at this temperature.

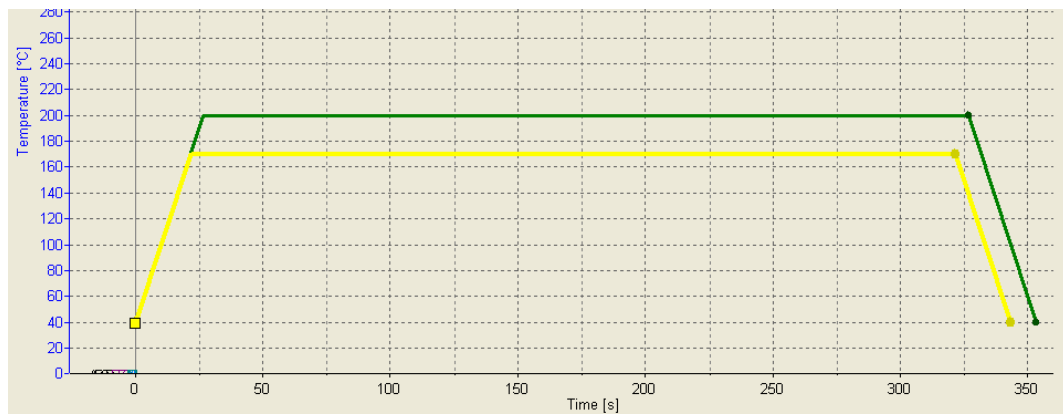


Figure 4.13: Thermal curing profile used during adhesive bonding

4.3.3 High Accuracy 30μm Pitch Assembly

Dies with 13μm bump were assembled on 8μm thick pads on the substrate leading to a stand-off height of around 20μm. The thickness of the adhesive film used was 25μm to ensure that the gap between the die and substrate was completely filled with adhesive during bonding process. Precise alignment of bumps to the bond pads on the substrate was done to ensure assembly yield at 30μm pitch.

The assemblies were one using $\pm 1\mu\text{m}$ accuracy Finetech Finaplacer tool, which requires that the sum of tool head length and die thickness be 22mm. Deviations from 22mm can lead to relative tilt in the die with respect to the substrate while placement resulting in partial yield during the assembly. This effect has been studied and reported in prior work, which outlined assembly yield for a die with peripheral bumps as shown in Figure 4.14.

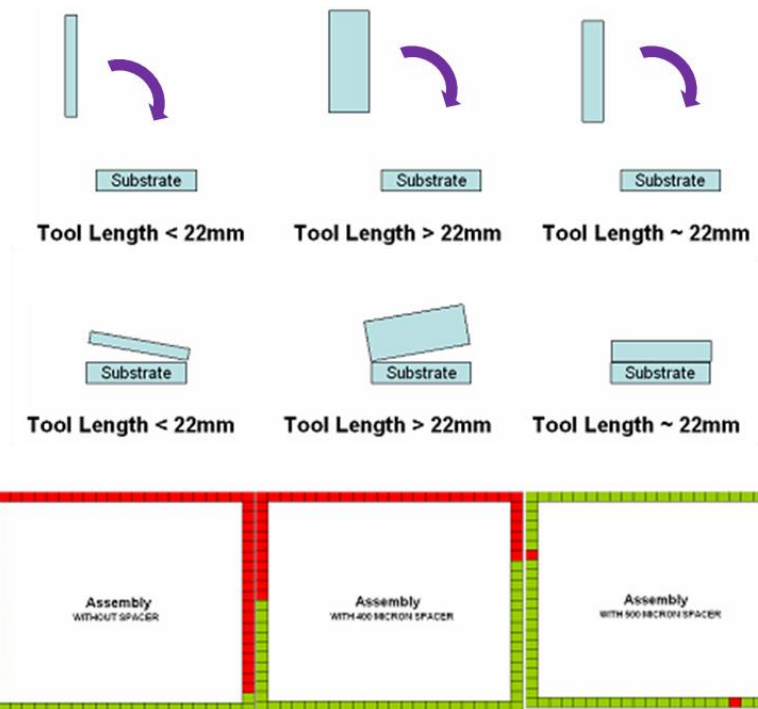


Figure 4.14: Effect of total length of tool head and die on the assembly yield [54]

The tool head used for all the test vehicles had a total length of 21.5mm which provided high yield assemblies for 550 μm thick dies assisted by the gimble in the tool head. But in case of 55 μm thin dies, the tool head was used along with 400 μm thick spacers to achieve similar yields.

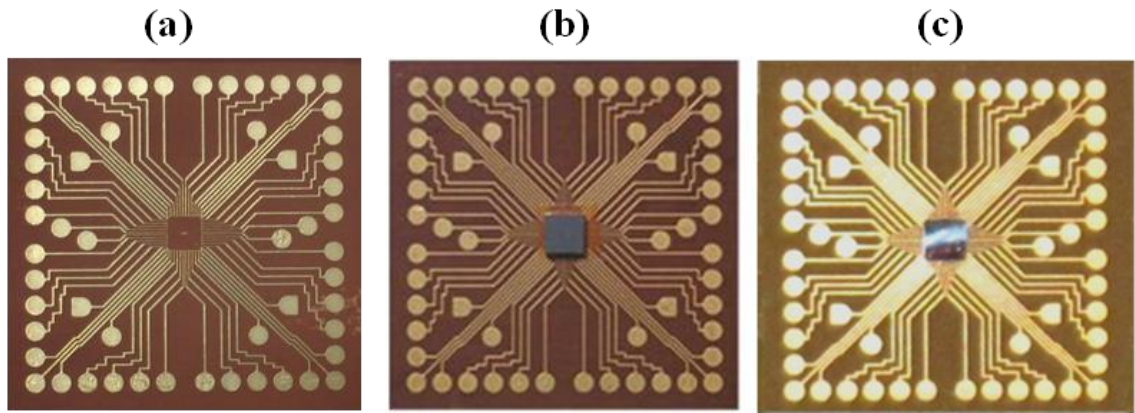


Figure 4.15: (a) One metal layer build-up substrate for TV1 (b) 550 μ m thick die assembled on the surface at 30 μ m pitch (c) 55 μ m thick die assembled at 30 μ m pitch

The snapshots of thick and thin dies assemblies for TV1 on the surface of the build-up substrate have been shown in Figure 4.15. Yield of the assembly was checked by probing the pads provided on the substrate for reading daisy chain resistance value. The accuracy of alignment of copper bumps to substrate pads was also inspected using X-ray imaging. Figure 4.16 shows the high accuracy of assembly process for 30 μ m pitch dies.

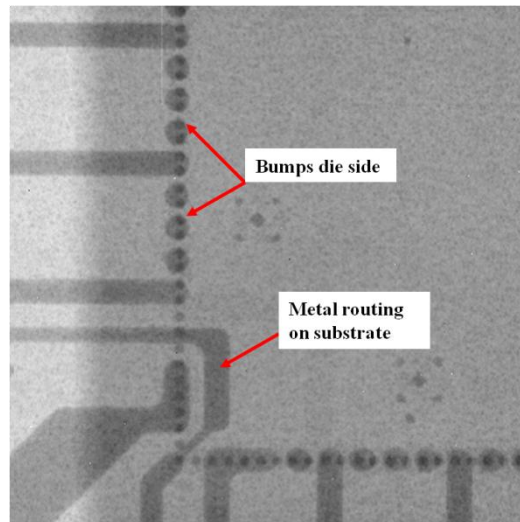


Figure 4.16: X-ray image showing accurate alignment of 30 μ m pitch copper bumps on substrate pads

4.3.4 Adhesive Bonding for Complete Embedding of Ultra-Thin Dies

The assembly process for embedding 55 μm thin die within the cavity posed several challenges. The handling and assembly processes were designed to prevent die cracking when subjected to thermo-compression bonding. Another challenge was to ensure a defect free NCF layer between the die and the substrate. As discussed earlier, cavity formation involved laser ablation of extra build-up layer to the dimensions of the cavity in all three directions. However, the build-up layer at the base of the cavity gets ablated to create a surface roughness as shown in Figure 4.17. Thus, the thickness of NCF was increased to account for such surface roughness and ensure a smooth flow in the gap between die and substrate. The size of tool head used for this assembly was also customized to transfer full load to the die as depicted in . The optimized assembly process yielded 55 μm thin dies being completely embedded within the cavity of the build-up substrate using adhesive thermo-compression bonding without any die cracking as shown in Figure 4.18.

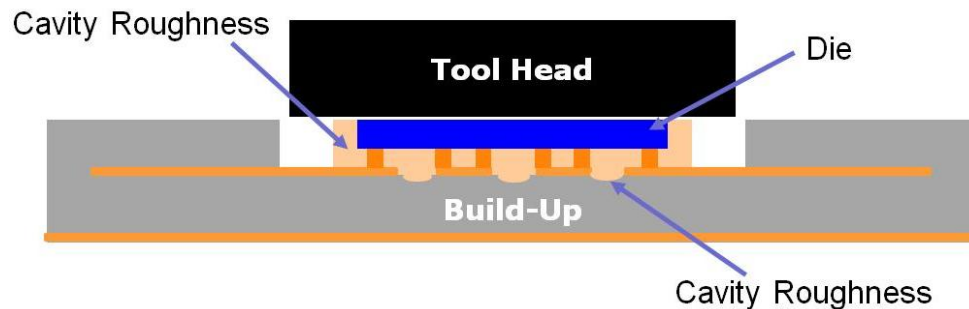


Figure 4.17: Schematic of assembly process inside a cavity showing proper size of tool head and NCF adjusted for surface roughness

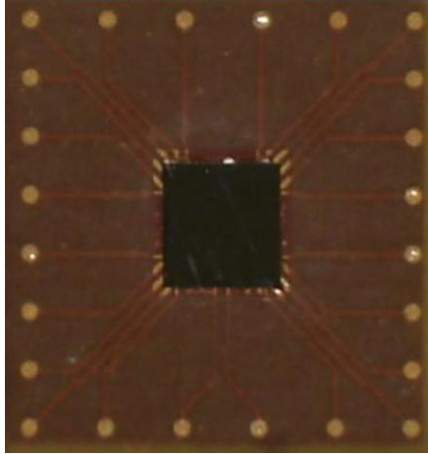


Figure 4.18: Image of thin die adhesively bonded within the substrate cavity

Uniform coverage of NCF was confirmed by C-SAM imaging as shown in Figure 4.19. The C-SAM images were used to check for any delamination of adhesive from die or substrate. Thin die was successfully embedded within the cavity with uniform NCF coverage and without die cracking as shown in the cross-section of TV2 in Figure 4.20.

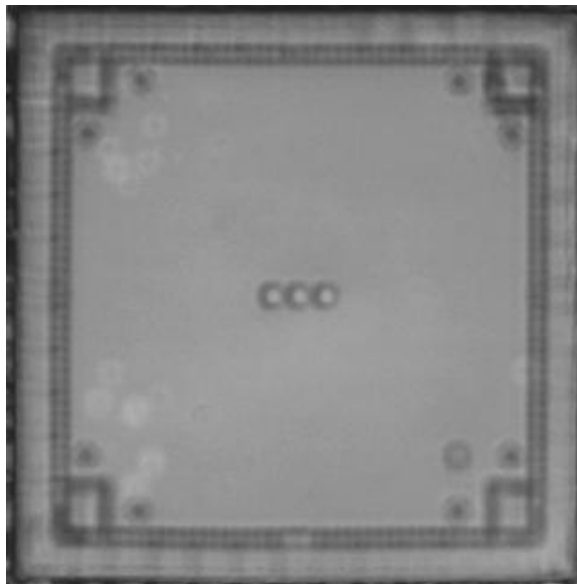


Figure 4.19: C-SAM image showing the die-NCF interface after thin die assembly within cavity

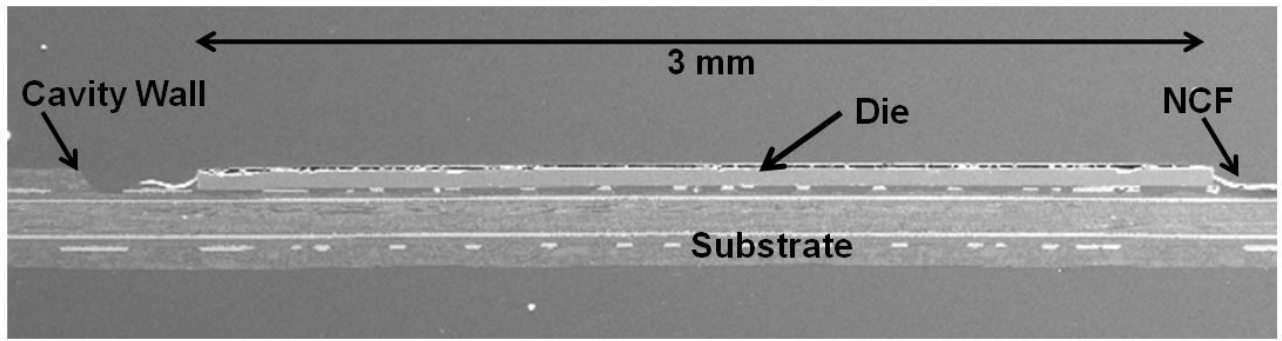


Figure 4.20: SEM image of cross-section of TV2 showing thin die embedded with the substrate

4.4 Contact Resistance of Single Copper-to-Copper Interconnection

Chung et al. has discussed the measurement technique for obtaining contact resistance of single bump interconnections using Kelvin four-point probe methods in case of NCF bonded packages. A simple schematic showing the setup for four-point probe method is shown in Figure 4.21. In this setup the first and second Cu lines are connected for the constant current (I) flow and third and fourth Cu lines are connected to measure the voltage (V). By using the Ohm's law, contact resistance can be calculated as $R = V/I$. In practice, the resistance value is calculated by finding the slope of the straight curve for voltage versus current.

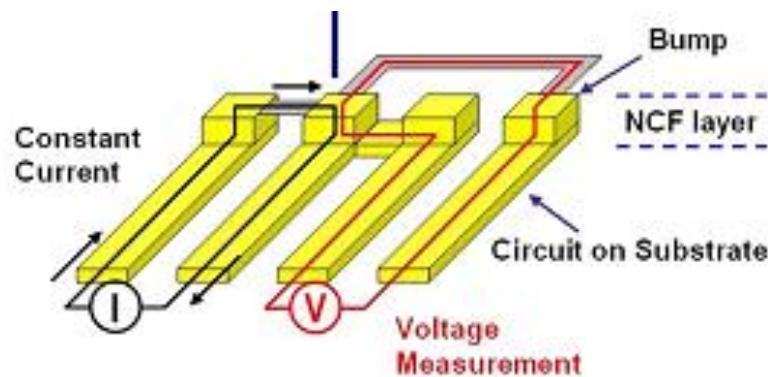


Figure 4.21: Contact resistance measurement of single bump by four-point-probe method

Single bump resistance values were measured for ~20 bumps across different TV1 samples assembled with NCF. The measurement was performed for corner bump of TV1 by Kelvin four-point probe method. Fixed current from 0.02-0.1A in steps of 0.02A was passed through the copper leads to read the voltage drop across the bumps. The resistance was calculated by averaging four readings per bump. The average contact resistance value obtained was ~7.55mΩ with minimum value as ~1mΩ and maximum as ~18mΩ. Based on the experimental resistivity data reported by Mhiaooui *et al* [61], compares the estimated resistance values of TV1 interconnect if it was to be replaced by different materials with same dimensions. It is evident from Table 4.3 that Cu bump interconnect with NCF provides better connection in terms of electrical resistance than most solders by lowering the parasitic resistance of the interconnect.

Table 4.3: Estimated contact resistance values if similar interconnections were made with different materials with similar dimensions

Interconnect	TV1	Cu	Sn ₉₉ Cu ₁	Sn ₉₆ Ag ₄	Sn ₆₀ Pb ₄₀
Resistivity (μΩcm)	-	1.7	49	50	60
Estimated Contact Resistance (mΩ)	7.55	1.2	33.3	34	40.7

4.5 Thermo-mechanical Reliability of Copper-to-Copper Adhesive Interconnects

The thermo-mechanical reliability of ultra-fine pitch copper-to-copper interconnections was studied using three industry standard tests used for qualifying any new interconnections technology as described in earlier. Previous attempts to realize such adhesive interconnections at fine pitch have been shown to have severe failure in U-HAST when assembled on glass substrates [54]. TV1 was used to improve the properties of adhesive by using additives to promote adhesion and inhibit corrosion. Exhaustive

reliability testing was performed to understand the root cause of failure in each test to improve the performance of interconnections on organic substrates. A summary of reliability testing performed on each test vehicle have been given in Table 4.4.

Table 4.4: Summary of reliability testing performed on each test vehicle

Test Vehicle	Reliability Test Performed
TV1	U-HAST/ HTS/ TST
TV2	TST
TV3	TST

4.5.1 Unbiased Highly Accelerated Stress Test (U-HAST) Performance

U-HAST test is conducted at elevated humidity and temperature conditions without biasing the interconnections during the test. High humidity and temperature are expected to degrade the interfaces in an adhesive joint causing local delamination, cracking at joints, hygroscopic swelling and corrosion of metallic interfaces. Moisture induced hygroscopic swelling has been reported extensively as a cause of failure for conductive and non-conductive adhesive based interconnections under humidity testing [43, 62-64]. Thus U-HAST serves as the most stringent test for studying the effect of high moisture on adhesive joints. Daisy chain resistance reading was taken as baseline measurement before subjecting the samples for testing. The samples were checked for open connections by measuring daisy chain resistance after MSL3 pre-conditioning, after 96

hours and after 192 hours of test. C-SAM imaging was used to monitor the interface between the die and adhesive.

Dies assembled on organic build-up substrate using NCF did not show any failure related to hygroscopic swelling after 192 hours of U-HAST. The C-SAM images shown in Figure 4.22 clearly indicate that the samples did not experience any moisture ingress or delamination even after 192 hours of U-HAST testing. This is contrary to results obtained earlier for dies assembled on glass which showed heavy moisture ingress and delamination even after 5 hours of test, showing that the NCF has better adhesion with organic build-up material as compared to glass.

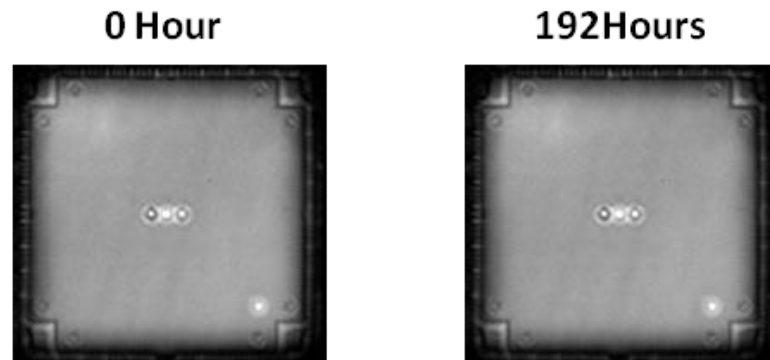


Figure 4.22: C-SAM images of TV1 under U-HAST test at 0 hour and after 192 hours. Both Cu finish and ENIG coated samples showed no moisture penetration but the increase in daisy chain resistance for Cu finish samples was ~4-5x of the increase for ENIG finish samples. The resistance values for ENIG coated samples with organic substrate showed only marginal increase till 192 hours of U-HAST as can be seen from Figure 4.23.

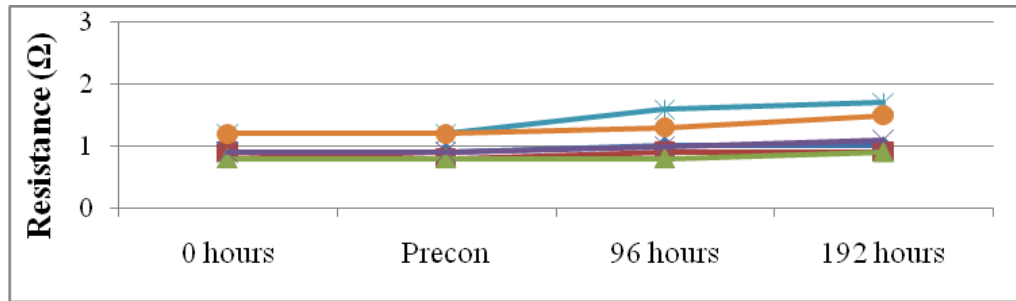


Figure 4.23: Change in daisy chain resistance during U-HAST for TV1 at 21N load

To study the effect of applied load on the reliability of copper interconnections, dies were assembled at 14N as compared to 21N load used earlier. The U-HAST result for dies assembled at 14N is shown in Figure 4.24. There is minimal difference in the performance of parts assembled at different loads, showing that both the loads- 14N and 21N were appropriate so as to not affect the reliability performance during U-HAST.

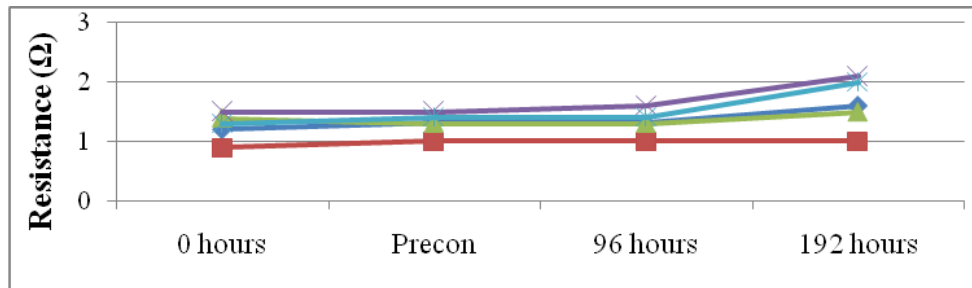


Figure 4.24: Change in daisy chain resistance during U-HAST for TV1 assembled at 14N load

The bumps located at the corners of the die have maximum impact of stress testing owing to their maximum distance from the neutral point (DNP). To assess the impact of U-HAST on the bumps with maximum probability for failure, single bump resistance from Kelvin test structures located at the corners of the die was also monitored. Figure 4.25 shows the individual bump resistance change during U-HAST for 20 bumps across various TV1 samples. The plot shows marginal increase in single bump resistance. In

addition, at the end of U-HAST test (96 hours), the average resistance is $\sim 31.66\text{m}\Omega$ which is still less than or comparable to most solders shown in Table 4.3.

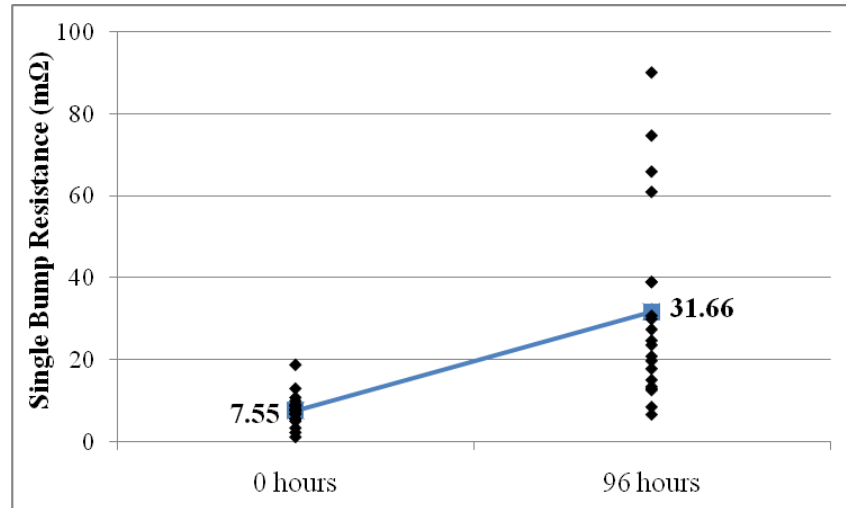


Figure 4.25: Change in single bump resistance during U-HAST for 20 bumps across different TV1 assemblies with NCF

4.5.2 High Temperature Storage Test Performance

Dies assembled at $30\mu\text{m}$ pitch were subjected to HTS testing at 175°C for 72 hours. The samples exhibited no failures during the test. The results compiled for 24 daisy chains from all the assemblies are shown in Figure 4.26. The resistance values shown in the plot were normalized and change in average value has been shown.

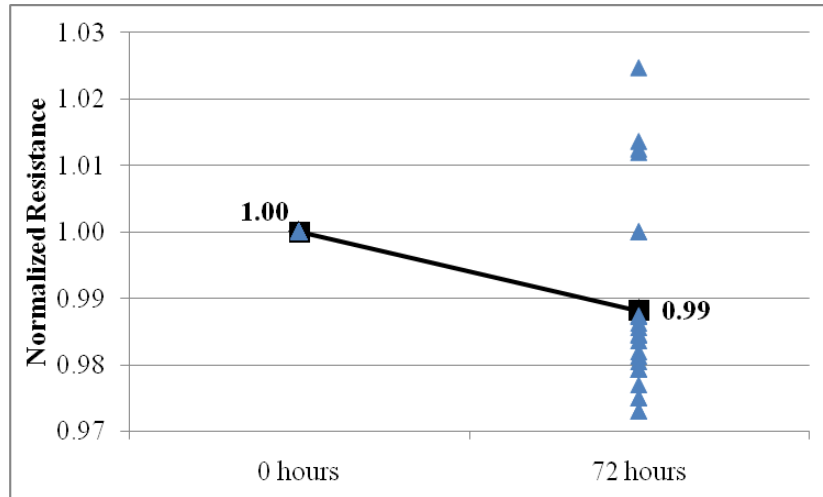


Figure 4.26: Normalized daisy chain resistance change during HTS for 24 daisy chains
The resistance change was within ~3% of the as assembled resistance. In addition, it is evident from Figure 4.26 that a decrease in resistance was observed for most of the daisy chains. This reduction in resistance could be attributed to further curing and shrinkage of the adhesive materials during HTS leading to improved connection between the copper bumps and pads.

4.5.3 Effect of Thermal Shock Testing on Copper Interconnections

Thermal shock testing is considered to be an aggressive test to assess the thermo-mechanical performance of electronic packages. Extreme temperatures seen by the package causes alternating expansion and contraction of individual components of the package based on their CTE. Differential expansion and contraction of die, substrate and interconnections cause cyclic stress within the package deteriorating the interconnections after prolonged temperature excursions. The test vehicles assembled with copper-to-copper interconnections with NCF were tested via TST with the tests being conducted using air-to-air thermal cycling till failures were seen. Daisy chain resistance was

measured every 100-150 cycles to monitor the performance of interconnections. The results of TST and discussion on failure analysis will be presented in the upcoming sections.

TV1 was assembled in two configurations with two different die thicknesses as shown in Figure 3.4. The first set of assemblies, done using 550 μ m thick dies were shown to have excellent reliability under HTS and U-HAST with highly stable bump resistance values comparable to its solder counterparts. Following this, TV1 samples were assembled using both 550 μ m and 55 μ m thick dies on similar organic substrates for testing their performance under TST.

TV1 with 550 μ m thick die

All the samples showed negligible change in daisy chain resistance values till 1500 cycles. The daisy chain resistance values obtained at every 100 cycle for some of the samples has been shown in Figure 4.27.

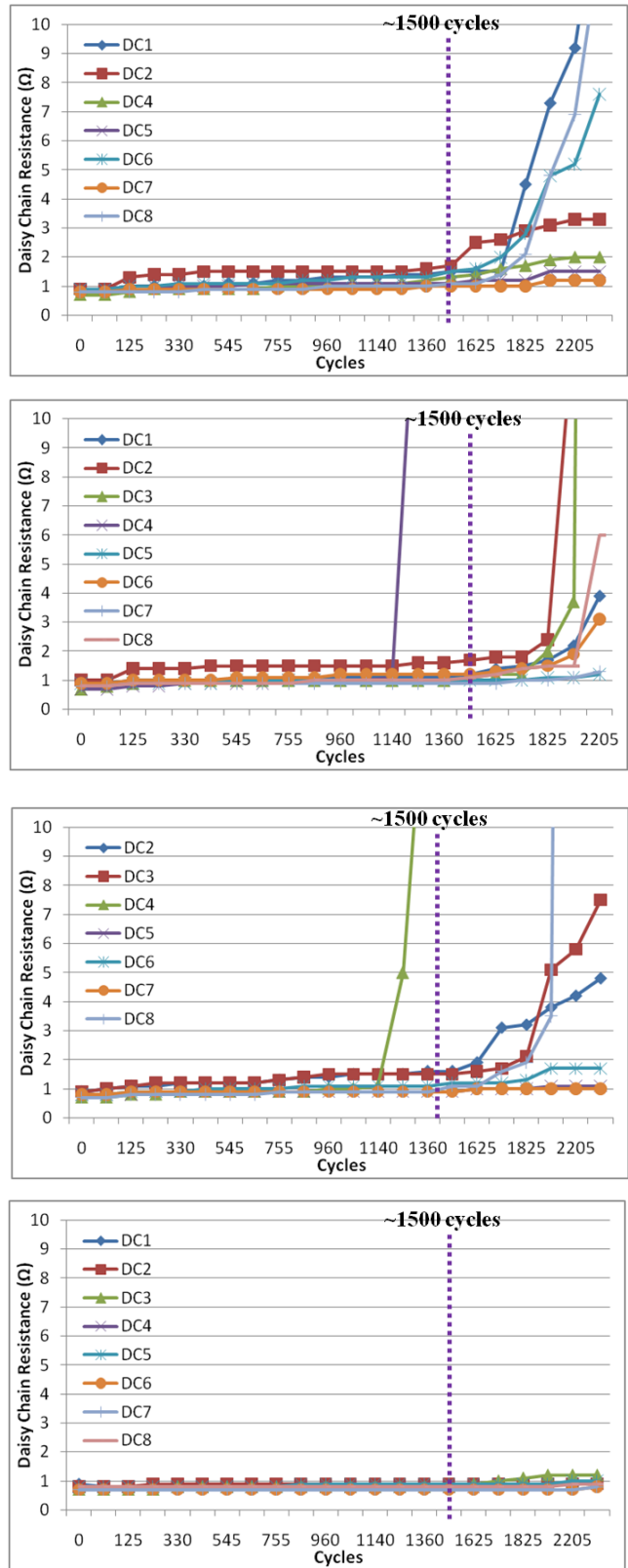


Figure 4.27: Daisy chain resistance values under TST for TV1 with 550μm thick die

The results indicate that the all the samples passed 1500 cycles of TST with failures observed at different points during the testing. Some samples showed excellent reliability through 3800 cycles with marginal increase in daisy chain resistance as shown in Figure 4.28.

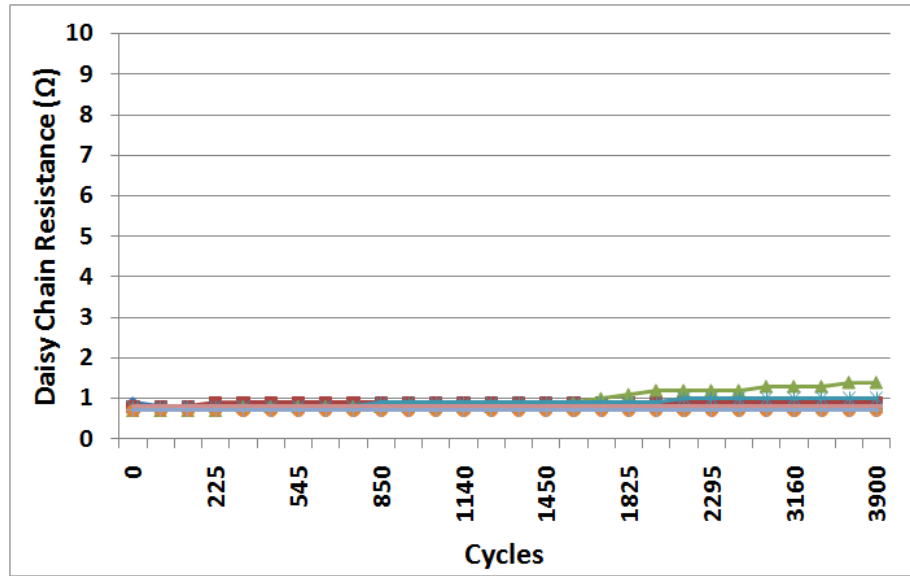


Figure 4.28: Daisy chain resistance values through 3900 cycles for 30μm pitch Cu-Cu interconnections

The failed daisy chains were cross-sectioned and prepared for SEM imaging to study the failure mode. For comparison between a working daisy chain and failed one, a working daisy chain after more than 2000 cycles of TST was also cross-sectioned to confirm the copper-to-copper interconnections. The interface of each bump-pad connections was examined under the SEM to understand the functioning of adhesively bonded interconnections. Figure 4.29 shows the cross-section of a working daisy chain of copper-to-copper interconnections. A magnified image of single copper-to-copper interconnections bonded using NCF is shown in Figure 4.30.

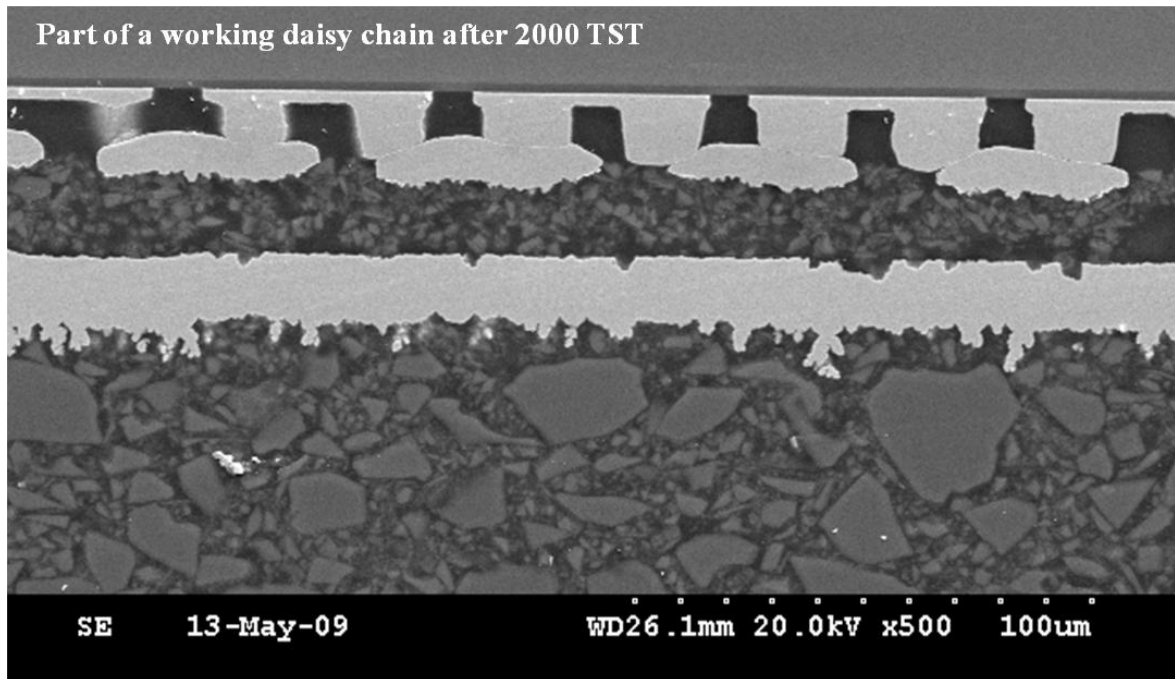


Figure 4.29: SEM image of a highly reliable working daisy chain of Cu-Cu interconnections

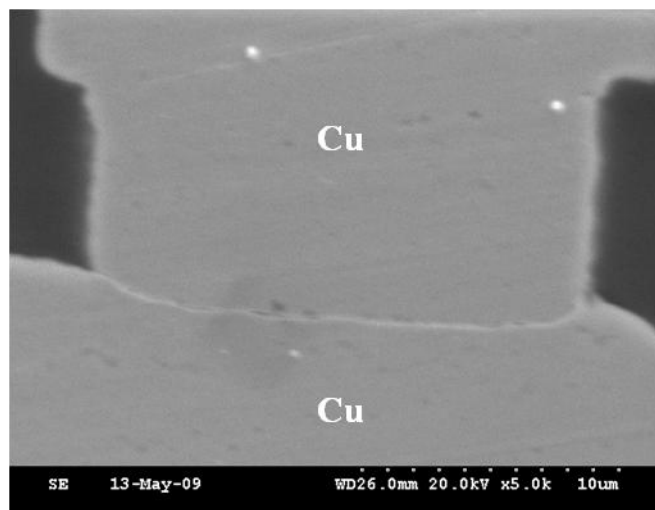


Figure 4.30: Single Cu-Cu interconnection using NCF

Some samples showed significant increase in daisy chain resistance or open connections after 1800 cycles shown in Figure 4.27. These samples were investigated for mode of failure as shown by cross-sectioning. Figure 4.31 shows a cross-section of a failed daisy chain after 1995 cycles. After closer inspection, the failure was identified to be due to

open connection at the bump-pad interface as shown in Figure 4.32. Similar failure modes were seen in other daisy chains which failed during TST as shown in Figure 4.33 for a daisy chain that failed after 2200 cycles. The study of bump-pad interface for non-failed and failed daisy chains indicates that failures seen during TST can be attributed to the pulling apart of the bump and pad causing physical separation between them, which leads to open electrical connections during the test.

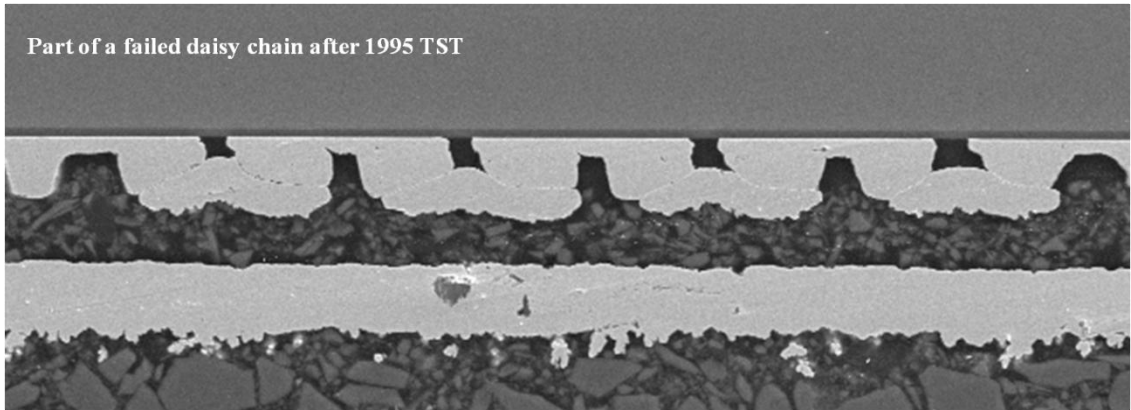


Figure 4.31: SEM image of a failed daisy chain after 1995 cycles

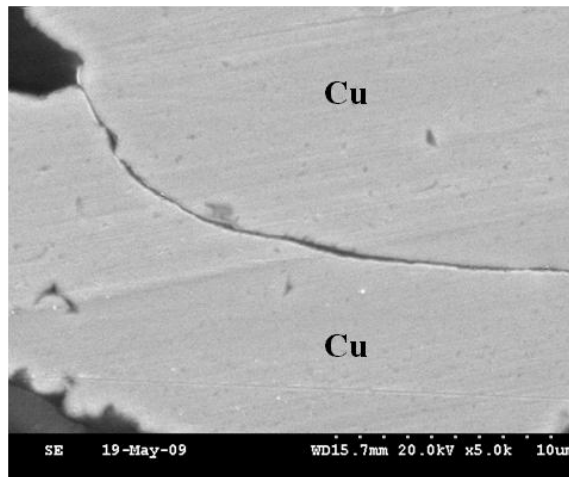


Figure 4.32: Magnified image of a failed bump-pad interface

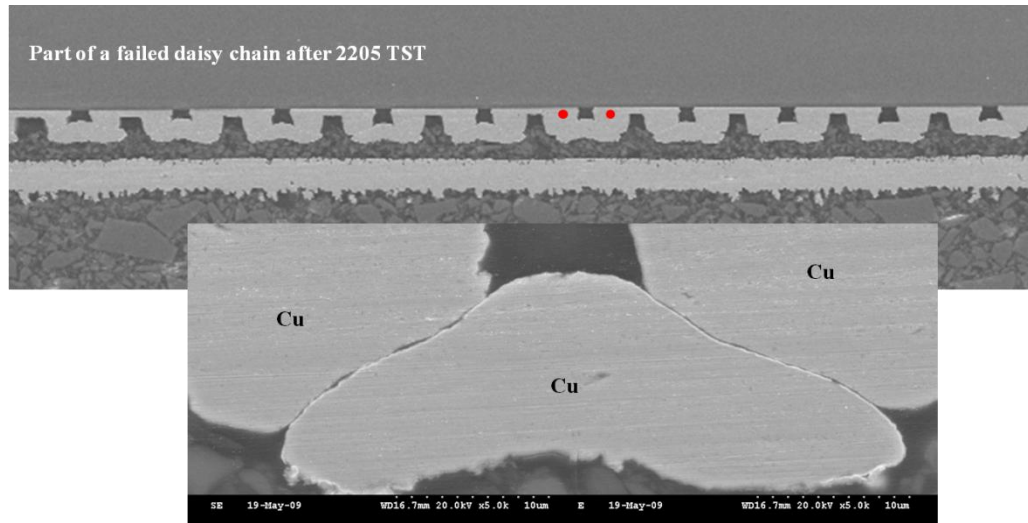


Figure 4.33: Failed daisy chain showing (inset) open connections at bump-pad interface

TV1 with 55 μ m thick dies

The assemblies with thinned dies also passed more than 1000 cycles of TCT, the results of which are shown in Figure 4.34. The TCT results in Figure 4.34 do not include daisy chains which did not yield at the start of TCT.

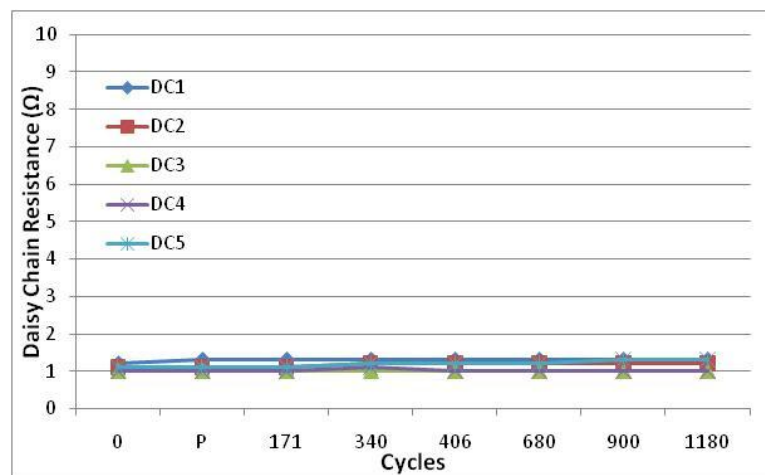


Figure 4.34: Daisy chain resistance data for TV1 with 55 μ m thick dies during TST

The assembly process for thinned dies was optimized to ensure that a load of 300MPa was applied to the copper bumps without damaging the die itself. The reliability results confirmed the appropriate process conditions for the assembly of 55 μ m thin dies.

Reliability of 55 μ m thin embedded die within the cavity

Reliability performance of copper interconnects was found to be highly dependent on the assembly process for embedding 55 μ m thin dies completely within a 65 μ m cavity in the substrate. As explained earlier, the tool head used for applying pressure during thermo-compression bonding was customized to ensure uniform load is transferred to the bumps equivalent to 300MPa. Figure 4.35 shows the impact of insufficient load during assembly of thin dies in the cavity on TST performance. The bumps were not seen to make enough contact with the pads and marginal deformation was seen in the bumps and pad.

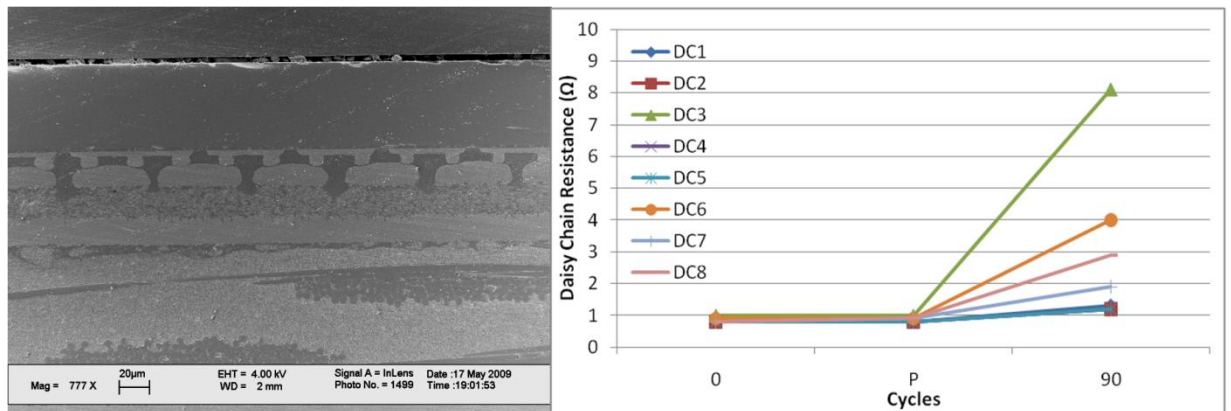


Figure 4.35: Failures seen in TST before assembly process optimization

After assembly process was optimized, all the samples showed stable daisy chain resistance under thermal cycling as shown in TST data for yielded daisy chains in Figure 4.36.

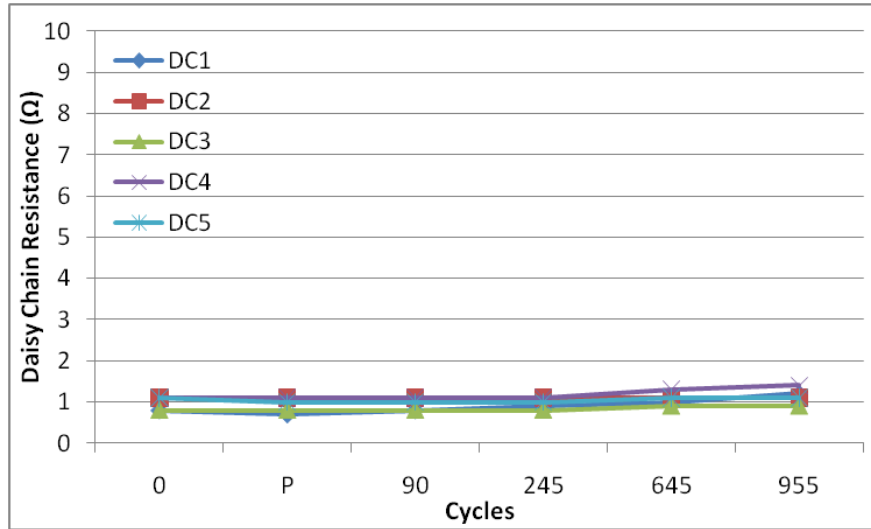


Figure 4.36: Daisy chain resistance data for TV2 under TST

Reliability of High I/O Large Die

The copper-to-copper interconnection was designed to be robust and perform well under different die thickness, die size and higher number of I/Os. In order to study the robustness of these interconnections in aforementioned conditions, $7 \times 7\text{mm}^2$ dies of $550\mu\text{m}$ thickness were assembled on the surface of the organic substrate (as shown in Figure 4.37) and evaluated for performance under TST.

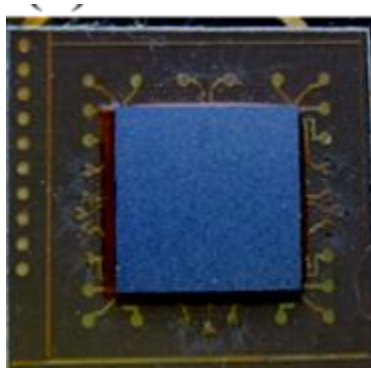


Figure 4.37: $7 \times 7\text{mm}^2$ die assembled on organic substrate using adhesive bonding

As mentioned earlier, this test vehicle included $7 \times 7\text{mm}^2$ dies with greater copper bump-to-pad contact area compared to $3 \times 3\text{mm}^2$ dies. Therefore, a higher load, calculated after taking into account the total contact surface of the bumps and pads was required to get sufficient deformation of bump and pad as shown in . Such deformations have been a signature of the assemblies, in TV1 and TV2, which showed good reliability under TST

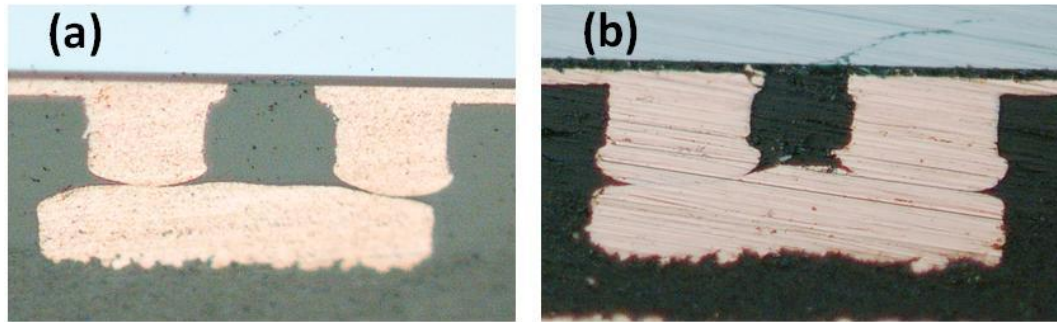


Figure 4.38: Optical image of the Cu bump on pad with an applied load of (a) 7kg (220MPa) (b) 9.5kg (300MPa)

The assemblies with higher applied load showed significant improvement in the reliability as shown by the TST results for samples assembled under 220MPa and 300MPa pressure in . The results indicate that higher deformation of bumps/pads improves the reliability of copper interconnections under TST.

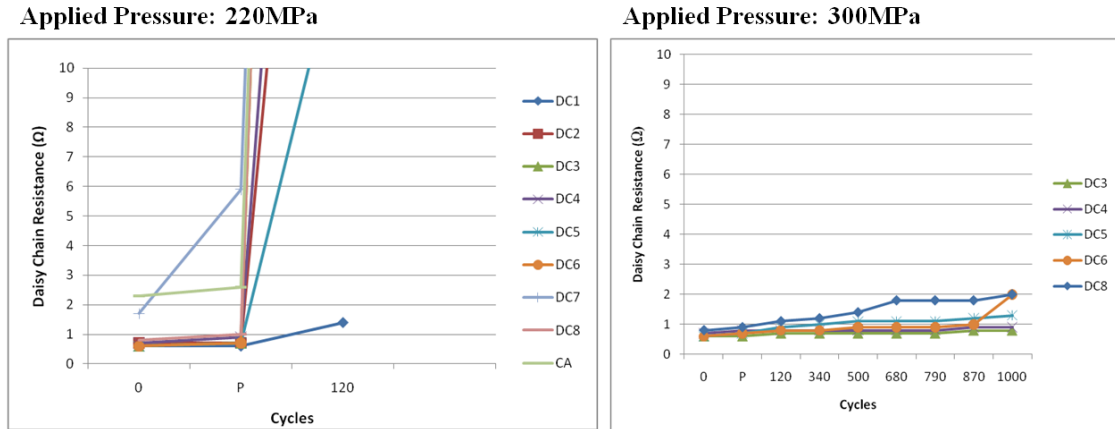


Figure 4.39: TST performance of 7x7mm² dies under 2 different applied loads for assembly

4.6 Morphological and Mechanical Properties of Fine Grained Copper Bump

The copper bumps used for ultra-fine pitch interconnects need excellent fatigue resistance and superior mechanical properties [65]. The desired material properties of interconnections closely depend on the fabrication process parameters as it can lead to altered grain structures and thus, different mechanical properties. To understand the effect of low current density on the properties of the electroplated copper bumps, the grain structure of copper bumps was studied using high resolution FESEM. As mentioned in the previous chapter, a low current density of 0.2-1A/dm² was used to electroplate copper for bump fabrication. The samples were ion polished to render mirror finish revealing the grain structure of copper. The Figure 4.40 shows the equiaxed grain structure of electroplated copper with grain size of less than ~300nm. Ibañez *et al.* has reported similar results on microstructural and mechanical properties of electrodeposited copper [66]. The study reports that the grain size of electrodeposited copper films is ~146nm for a current density of 0.6 A/dm². The results obtained from this study align

well with the values reported in the literature considering the copper bumps were annealed at 125°C for 1 hour which would lead to marginal grain growth.

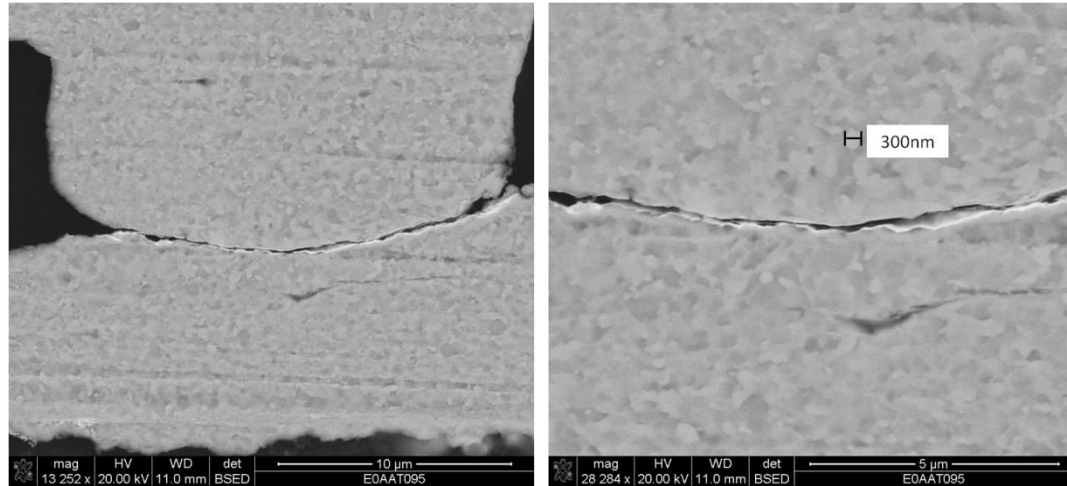


Figure 4.40: SEM image of ion polished copper bump

Ibañez *et al.* also reports that as the current density increases the grain structure refines until 12 A/dm² beyond which the refinement ceases. This directly affects the elastic modulus of the material based on the Hall Petch effect that establishes a linear dependency of the hardness with the reciprocal square root of grain size [67]. The reported value of elastic modulus for copper electrodeposits at such low current densities is 57±3 GPa.

4.7 Diffusion Study of Copper-Copper Interface

The bump-pad interface of copper-to-copper interconnections was studied for elemental diffusion across the interface. Such thermally assisted movement of mass across the interface would lead to a continuous metallurgical interface improving the bond strength of the joint. To understand the effect of adhesive bonding on the bump pad interface, cross-section of the bump-pad was studied using EDS technique. Line scans for elements

like Ni, Au, Cu and C were performed across the interface to study patterns of elemental composition across the interface. Figure 4.41 shows a plot of spectra obtained across copper-copper joint with ENIG surface finish. The spectra indicate that there is no significant diffusion occurring for Cu and Ni as the peaks for each were located as per their original positions in the joint. It is also evident from the plot that the interface is constituted primarily by gold on both sides indicating a gold-to-gold interface.

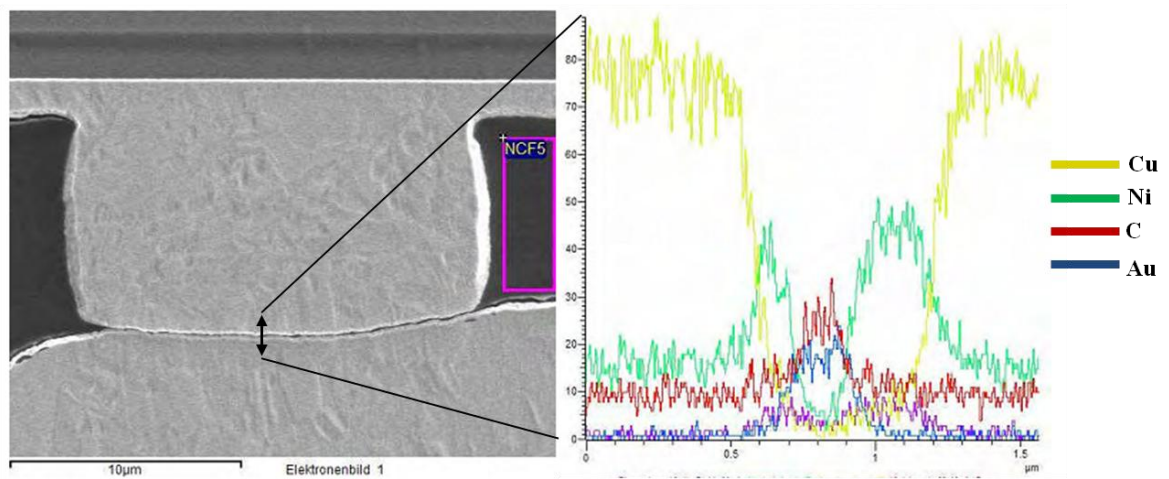


Figure 4.41: Plot of EDS spectra for Cu, Ni and Au obtained across the bump-pad interface (courtesy Infineon)

4.8 Proposed Hypothesis for Reliable Copper-to-Copper Interconnections

Adhesive bonding has been extensively reported for chip-on-glass substrate and chip-on-flexible substrate packages. Most of the reported literature involves use of ACF as adhesive which relies on entrapment of conductive filler particles with an increasing acceptance for non-conductive adhesive as a better solution for chip-on-flex application. Caers *et al.* has reported effects of cyclic stress loading on the contact resistance of a metal-to-metal bond formed using non-conductive adhesives [68]. According to this study, compressive stresses develop at the interface of the mating bumps due to shrinkage

caused by curing of adhesives. The magnitude of this compressive stress also referred to as “pre-stress” determines the initial contact resistance and is the key for a successful electrical performance. Also, the durability of the connections under cyclic thermal loading depends on the relaxation of residual compressive stresses due to viscoelastic properties of the adhesive.

The failures seen in copper-to-copper interconnections can also be explained well by this theory. The failures under cyclic load of thermal stress are caused due to mechanical separation of bump and pad indicating relaxation of compressive stresses induced due to curing of NCF. As seen earlier, low temperature of bonding could prevent diffusion across the bump-pad interface leaving the copper-to-copper interconnections as a non-metallurgical bonded interconnection. However, one of the key aspects of assemblies which showed excellent reliability under TST was that extensive deformation was seen in bumps and pads. The mechanical properties of electrodeposited copper vary according to the current density. Low current density plating of copper yields copper bumps with low elastic modulus which can deform much more than bulk copper. To gauge the extent of deformation seen when a 13 μm tall bump is deformed on the pads with 300MPa (pressure applied during assembly) a die was assembled on the substrate without NCF and the pad deformation was measured after manually detaching the die. **Figure 4.42** clearly shows that the pads on the substrate deform 2-3 μm in the z-direction during adhesive bonding process.

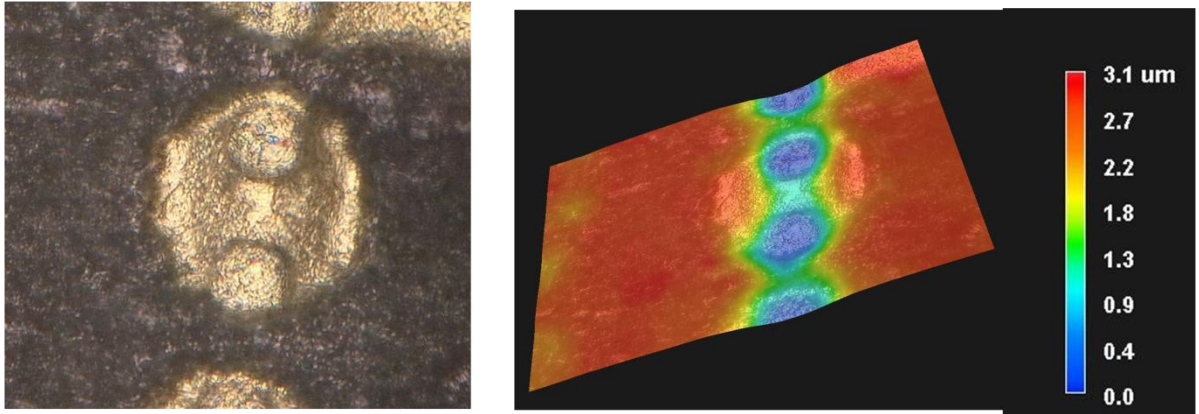


Figure 4.42: 3D rendered optical image of a deformed substrate pad showing extent of deformation

Such high degree of deformation can be contributed by the mechanical properties of electroplated copper and soft build-up layer on which the pads are fabricated. Despite the stress relaxation caused failures, the Cu-Cu interconnections showed excellent reliability beyond normally expected performance of adhesive bonded packages surviving more than 2000 cycles of TST. Such mechanical integrity could also be assisted by mechanical interlocking locally at bump-pad interface as seen in Figure 4.43.

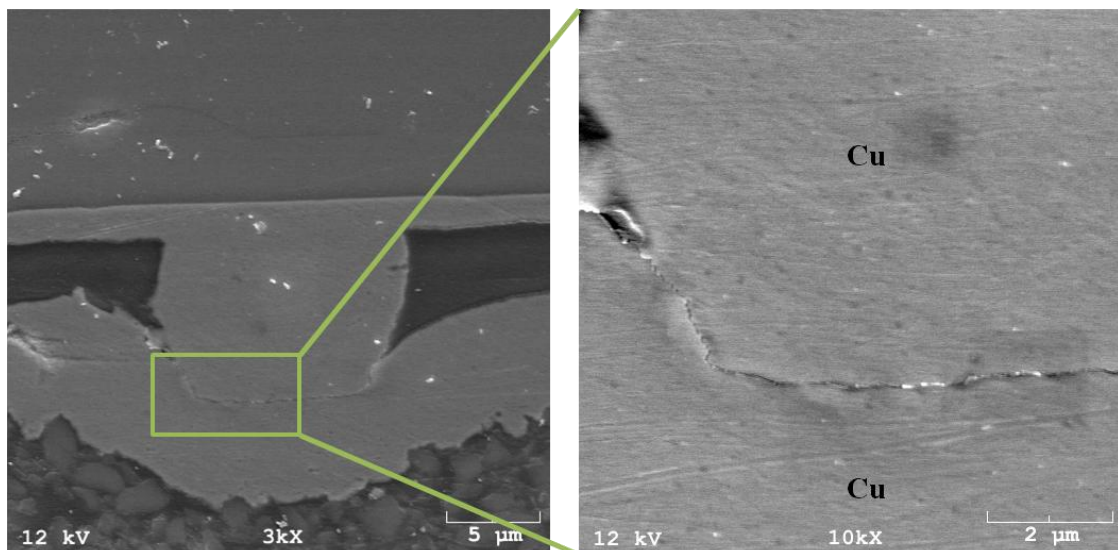


Figure 4.43: SEM image of Cu-Cu interconnection interface under extensive deformation

The measurement for daisy chain resistance during thermal shock testing was done at room temperature. This allows the copper and the surrounding adhesives to cool and shrink before the measurement is taken. As the Cu-Cu adhesive interconnection is believed to be a mechanical joint, it could be possible that the adhesives expand much more than the copper during heating leading to open connections at high temperature. These connections are again restored during cooling due to excessive shrinkage of adhesives compared to copper. To further validate this theory, in situ measurement of daisy chain resistance during thermal shock testing could be done. Open connections after prolonged testing could be again attributed to stress relaxation of adhesives which causes the compressive stresses, which hold the copper bumps against the copper pads, to decay and cause permanent separation between the bump and pad.

5. Conclusions and Future Work

This chapter presents a summary of various studies conducted as a part of this research and draws meaningful conclusions of the work. In later part of the chapter a list of on-going research and recommendations for future innovations is presented and discussed.

5.1 Conclusions

The microelectronic systems are evolving faster than ever to accommodate higher and higher degrees of functional integration on a single platform. Highly integrated mixed signal ICs requiring more than 10,000 I/Os need short and highly reliable interconnections for making their way to production. Clearly the demand for low profile interconnection technology is becoming the bottleneck for commercialization of thin embedded packages which are expected to see extensive application in wireless and portable consumer electronics market. Traditional eutectic solder based interconnection fast transformed to lead-free regime with the environmental regulations setting in. However, the reduction in pitch for these interconnects became a concern beyond 130-150 μ m leading to a consolidated effort by the industry to develop alternative solutions to further reduce the pitch and size of interconnections. Copper pillar was a paradigm which promises to go beyond the barriers of C4 solder interconnections giving excellent mechanical, electrical and thermal performance. Companies like Intel and TI are now shipping processor chips which are attached using copper pillar and solder. This technology possesses excellent potential for performing at fine pitch with 50-80 μ m pitch copper pillars being reported by various groups around the world. However, high stand-off height creates concerns about Cu/low k compatibility which could be aggravated for extra low k (ELK) and ultra low k (ULK) dielectrics. Such interconnections possess

reliability concern and solder mask limitations at even finer pitches. Alternative metallurgies using Au are being considered by the industry as an expensive solution with rising price of gold.

In the wake of standard flip-chip failing to sustain the requirements of next-generation high I/O packages, die embedding is emerging as an important solution. The ability to provide interconnections to greater number of dies at once due to wafer level or laminate level processing, keeps these packaged at lower end of the cost per I/O. Throughput of interconnections in these embedded packages can be improved significantly by using photo definable dielectric while maintaining extremely small dimensions. Such interconnections are being scaled down to 20 μ m pitch with improvement in process pushing it further down. However, low yielding processes which accumulate over the pre-committed die create a bottleneck in its use for large scale production.

The next generation of packaging technologies will need robust interconnection solutions which can support extremely high area array I/O count. The interconnections size needs to shrink significantly to almost reach pad-to-pad bonding at extremely finer pitch of 1-20 μ m. Such solutions have already started emerging for 3D Si integration with Si-to-Si being bonded at 5-10 μ m pitch. Several groups have reported of forming direct metal to metal bonding for fine pitch application but are limited by their scope due to complex manufacturing processes involved, high temperature requirements or high surface cleaning requirements. Thus simple low profile chip-to-organic package interconnections are needed for enabling future embedded packages which will integrate heterogeneous sub-systems.

In the present work, a novel architecture for achieving direct copper to copper bonding was demonstrated for the first time using adhesive bonding. This technology was used to demonstrate a new method of embedding active chips referred to as “chip-last” for realizing IC-to-package interconnection with chip-first benefits. This interconnection technology, in contrast to widely- pursued technologies such as chip-first or wafer level fan out with embedded IC, possesses superior attributes that include low-profile, high I/O density, low temperature bonding, testability and ease of integration with existing manufacturing facilities. Low profile interconnection, with a standoff height of less than 20 μm , is one of the key aspects of chip-last technology.

Copper bumps of 13 μm height were fabricated on silicon wafer with ENIG surface finish. Build-up substrate was fabricated for test vehicles designed for studying the reliability of copper-to-copper interconnections. Copper bumps on silicon die were bonded to copper pads on substrate using NCF at 160°C. The dies were assembled on the surface and within the cavity of the organic substrate. Single bump resistance of copper-to-copper interconnection was measured to be an average of 7.5m Ω which is less than or comparable to resistance of similar bump architecture with different solders. The test vehicles with 3x3mm² die showed excellent reliability under U-HAST, HTS and TST. Both thick die and thin die assemblies on surface and in the cavities showed excellent results in thermal cycling tests and maintained stable contact resistance during the test. The assemblies with larger die size of 7x7mm² passed more than 500 thermal cycles. These initial results with large dies indicate that these interconnections functions well with high I/O large size die too. The failure analysis revealed the mode of failure during TST to be physical separation of bump and pad indicating a non-metallurgical or

mechanical bond holds the bump and pad together. Also the excellent reliability of these interconnections can be attributed to extensive deformation seen in bump and pads leading to local surface interlocking.

It can be concluded that copper-to-copper interconnections using adhesives can be used to develop multichip embedded chip packages with heterogeneous dies at even finer pitches of 10-20 μm with extremely low stand-off height.

5.2 Recommendations for Future Work

This work has demonstrated a robust interconnection technology which promises to play an important role in defining the next-generation ultra-thin multi-functional packages. Achieving excellent reliability at ultra-fine pitch and extremely small dimensions was one of the key goals of this thesis. In order to push this technology for wider applications and ready for large scale productions several challenges still need to be addressed. Some of the innovative solutions currently in progress of this research and scope for fundamental study have been enumerated below:

- Copper-to-copper interconnections, with peripheral layout at 30 μm pitch, were shown to have excellent reliability. Currently this technology is being studied for reliability performance with large area dies with area array bumps. Assembly process, adhesive material and bump co-planarity need to be optimized for achieving similar reliability at 50-80 μm pitch of area array interconnections.
- These results of the study indicate formation of non-metallurgical or mechanical joint due to low temperature of bonding. For further improving the reliability, various methods of achieving metallurgical bonding can be explored along with adhesive

bonding. Thermo-sonic bonding, mostly used for gold-to-gold bonding, can be explored for improving the bump-pad interface. Novel thin-film solder can also be deposited as nano-particles on the surface of copper bumps to achieve metallurgical bonding.

- Thermo-compression bonding was done on single chip per assembly. This method becomes difficult to compete with high throughput flip-chip solder based assembly which can be batch processed. A breakthrough approach is currently being developed for increasing the throughput of copper-to-copper interconnection based embedded. Several dies are aligned and placed in substrate cavities on a panel followed by gang bonding at panel level to yield higher number of assemblies. This multi-chip panel level approach can reduce the assembly time by 10X from 30seconds to ~3-5 seconds based on number of dies per panel.
- Lastly, as this interconnection technology is matured, a thorough study of effect of these interconnections on low-k, ELK and ULK dielectric materials needs to be done. Mechanical models accurately predicting the stresses transferred to the Cu/low-k structures should be developed and validated.

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